Optimierung von Übertragungseigenschaften in UHF-Transpondersystemen

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I dedicate this thesis to my family, specially to my wife Senta, whose support helped me over last 3 years of hard work and challenges. To my tutors and colleagues for guiding me in the rough road a PhD pursuit can be.

Abstract

This work presents optimizations and improvements for UHF RFID systems which increase the system sensitivity, as well as the successful read attempts on harsh environments. A basic system description and analysis are displayed followed by the description and test of the new approaches. The considered system elements are: encoding, receiver architecture, digitization of RF signals, carrier suppression, information recovery and system prototyping.

Contents

List of Figures

List of Tables

Nomenclature

f_s ..... Sample Frequency
f_{max} ..... Maximum Frequency Limit
f_{min} ..... Minimum Frequency Limit
ADC ..... Analog Digital Converter
BER ..... Bit Error Rate
BLF ..... Backscatter Link Frequency
CIC ..... Cascade Integrator Comb
CW ..... Continuous Wave
DAC ..... Digital Analog Converter
dB ..... Decibel
dBc ..... Decibel to carrier
dBm ..... Decibel milliwatt
DC ..... Direct Current
DSB-ASK ..... Double Side Band - Amplitude Shift Key
DSP ..... Digital Signal Processing
EAS ..... Electronic Article Surveillance
ERP ..... Effective Radiated Power
FFT ..... Fast Fourier Transform
FIR ..... Finite Impulse Response
FPGA ..... Field Programmable Gate Array
GSPS ..... Giga Samples per Second
I-Q ..... In-phase/Quadrature
IC ..... Integrated Circuit
IF ..... Intermediate Frequency
ISI ..... Inter Symbol Interference
ISM ..... Industrial, Scientific and Medical

ITU ..... International Telecommunication Union
LO ..... Local Oscillator
ML ..... Maximum-Likelihood
MSPS ..... Mega Samples per Second
PA ..... Power Amplifier
PCB ..... Printed Circuit Board
PI ..... Proportional Integrator
PLL ..... Phase Locked Loop
PN ..... Pseudorandom Noise
PR-ASK ..... Phase Reversal- Amplitude Shift Key
PWM ..... Phase Wave Modulation
RFID ..... Radio Frequency IDentification
RUT ..... Reader Under Test
SNR ..... Signal to Noise Ratio
SRD ..... Short Range Devices
SSB-ASK ..... Single Side Band - Amplitude Shift Key
UHF ..... Ultra High Frequency
VGA ..... Variable Gain Amplifier
VHDL ..... VHSIC Hardware Definition Language
VHSIC ..... Very High Speed Integrated Circuit
W ..... Watt

Chapter 1

Introduction

1.1 Motivation

Radio frequency identification (RFID) systems use radio waves in order to retrieve the identity of an object. They are grouped under the broad category of automatic identification technologies. Unlike bar-code technology, RFID technology does not require physical- or optical contact for communication. RFID data can be read through the human body, clothing and non-metallic materials.

The main parts of an RFID system are: the reader which manage the communication and the tags which are the identifiable devices attached to objects. RFID systems are basically divided into active and passive. In passive systems the tags use the energy of the electromagnetic field radiated by the reader as energy source and as carrier for the data transmission. Active tags are provided with energy by local means. The RFID systems work in LF, HF, UHF frequency bands [29].

In the last years RFID has evolved into an active multidisciplinary area of research and development, composed by a broad spectrum of fields. The tasks of RFID tags have become more complex, this includes:

- Tags that are placed in reflective environments.
- Tags that are provided with sensor capabilities used to monitor specific processes.
- Higher data rates are needed in systems where the tag sends more than just its ID, i.e. sensor tags [17].

- The reliability of RFID systems has to be increased. The user needs to be sure that all tags are read at all times.

All these challenges open the doors for research and development in the areas of RFID [34]. Many algorithms and technologies of other communication areas can be applied to RFID systems. The goal is to optimize and improve the RFID Systems. This work focus in RFID passive systems working on the UHF frequency band.

1.2 Problem

RFID systems working in UHF band use electromagnetic waves to communicate with the tags. There are certain channel characteristics that affect the communication when working at high frequencies. The electromagnetic waves are reflected by objects in the surroundings creating a *multipath effect*. In other words different waves arrive at different points in time and with different magnitudes. This effect has a direct influence on the energy available at the tag, and therefore on the information signal transmitted by it.

Mobile reflective objects in the surroundings of the tag create a dynamic transmission channel. In this case the multipath effect generates fluctuations of the available energy at the tag, this effect is called *fading effect*. This effect can create inter-symbol interferences in the transmitted data. The fading effect creates gaps in the field distribution where there may be not enough energy available for the tag to operate properly.

Another known problem in RFID systems is the carrier overlapping. Due to the fact that the carrier is used for powering the tag, it is present in the receiving process as well. A big amount of the carrier leaks into the receiving path thus increasing the complexity of the data recovering.

All these effects have a direct influence on the signal received by the reader, this complicates the recovering of the information contained in the signal.

There have been several studies over the channel influences in UHF RFID systems, nevertheless only few have presented results over the influence on the baseband signal, see [25], [13], [18], [40], [56], [30], [48]. This work presents how the different channel effects influence the baseband signal and some algorithms to increase the data recovery rate.

1.3 Goals

Successful Reading in Adverse Environments

The goal is to enable or even increase the probability of a successful read in harsh environments. Further more the new algorithms increase the read range as well.

Adaptive Algorithms

The working conditions of the RFID systems are not static (e.g. dynamic channel, moving objects) and every application imply a different challenge. The new algorithms should adapt to the dynamic working conditions.

Configurable Reader

Another goal of this work is to design a UHF RFID system that works with the new algorithms and fulfills the goals already presented. This system can be used as a prototyping and test environment platform. This platform should be as flexible as possible in order to be able to use the same system for different applications.

1.4 Scope

The following diagram on Figure 1.1 presents an overview of the main elements in an UHF RFID system. The gray shadowed blocks represent elements in the system considered by this work and where new approaches or improvements are presented. The details of these elements are presented in chapter 5. The white blocks are standard elements in the system which are needed to complete the system.

Encoding: A new line coding scheme is presented which presents a more robust behavior on harsh environments compared to the standard scheme. The new coding scheme takes advantage of the orthogonality between symbols which increases the data rate as well.

Carrier Suppression: The carrier leakage in the receiver path is one of the most critical problems in UHF RFID, it has a direct influence in the sensibility of the system. Hence a new carrier suppression circuit and its controller are introduced in UHF RFID. The new approach increases the carrier isolation, hence decreasing the carrier leakage

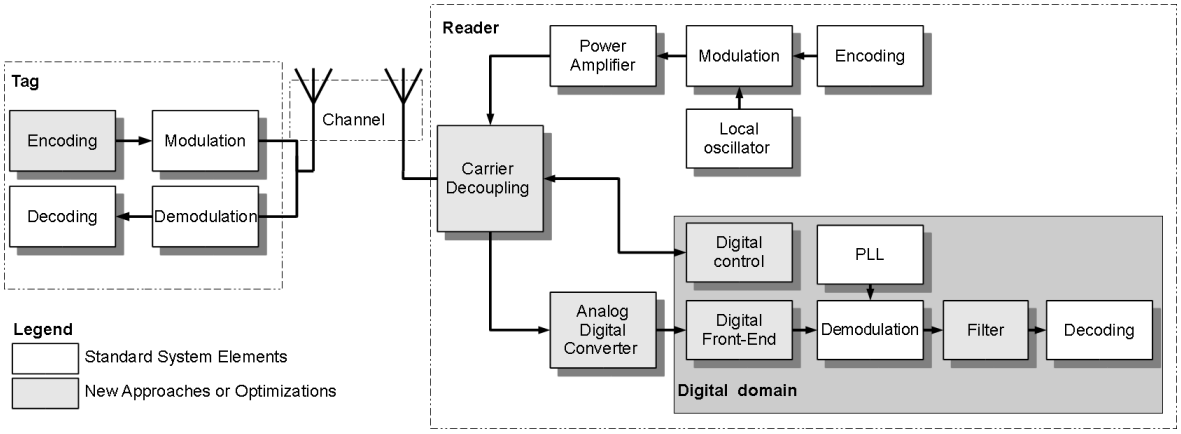

Figure 1.1: Thesis Overview Presented as Block Diagram

on the receiver path, furthermore the SNR of the signal is improved as well. Due to its extension the details of the system are presented in chapter 6.

Digital Domain: The first approach of this work is to implement most of the signal processing in the digital domain. The digital domain is represented in Figure 1.1 as a big gray block, all the elements inside this block are defined by software. In this case the white elements are standard components in the system which tasks are typically made by analog circuits.

Analog Digital Converter: An under-sampling is scheme is used to digitize the RF signal directly, without the need of frequency translation.

Digital Front-End: A digital front-end was developed in order to pre-process the under-sampled signal before the demodulation.

Filter: The receiver filter is extended to the complete length of the Miller codes. Using long Miller codes in connection with receiver filter increases the reliability of the data recovering.

Chapter 2

Background

This chapter presents the basics of an UHF RFID system, its components, characteristics and applications areas. Some basic concepts on analog to digital conversion for UHF RFID systems are presented as well.

2.1 UHF RFID Systems

The use of the UHF band in RFID has been increasing in the last years, the market worth has reach $900 million in 2011 according to ABI research [5]. It enables the user to read tags at distances up to 6 meters [29]. This technology has opened the doors for new application fields, especially in the logistic. The use of RFID technology in UHF band is standardized by the EPGGlobal Class 1 Gen1 and Gen2 standard [27].

2.1.1 Description

A basic UHF RFID system consist of three parts:

- *Reader*: It controls all the communication activities and generates the electromagnetic field to power the tag (for passive systems).
- *Tag*: It is an identifiable element in the system. It can be attached to any object that needs identification.
- *Information System*: It manages the information obtained by the reader. Data banks, information management, control, etc.

Characteristics

- The UHF RFID systems use the SRD (Short Range Devices) frequency band (860-960 MHz).
- They are characterized for its potential long range.
- The relative simplicity of the UHF antenna designs helps to reduce the cost of fabrication [24].
- The UHF tags have been used especially in the logistic where its relative long range adds flexibility to many tasks.

Application Areas

- *EAS (Electronic Article Surveillance) and Inventory*: One of the biggest implementation area of UHF RFID is the clothing sector. RFID tags are used for item inventory and store surveillance.
- *Supply Chain Management*: The UHF RFID tags are used to identify elements in the supply chain. The items need not to be actively controlled, their iterations are monitored by readers that can be installed in gates or directly in the transport bands.
- *Transport Tracking*: The inventory of the elements in a transport vehicle can be done by readers mounted in a gate where the vehicle pass through.
- *Sensors*: A relative new and still in development application, is the use of UHF RFID tags to passively monitor environment variables such as temperature, humidity, pressure etc. The passive tags can be placed in objects that require some special environment conditions and monitor them. It is in this application where the need of a more robust system comes afloat. The sensor-tags may need to be placed in objects that have direct influence on the transmission channel [17].

2.1.2 Tag

The basic construction of the UHF RFID tags consist in a dipole antenna that is used to gain energy out of the electromagnetic wave and at the same time to send the data back to the reader. The main part of the tag is an integrated circuit (IC) that contains:

- *Voltage Supply*: The circuitry necessary to generate a stable voltage out of the electromagnetic wave in order to supply the tag's logic.

- *Demodulator*: The circuit that obtains the information signal out of the high frequency carrier.

- *Modulator*: The circuit used to send the information back to reader by changing the impedance of the antenna.

- *Protocol Stack*: A state machine that is responsible of the communication protocol.

- *Memory*: A certain amount of memory where the tag's ID and other information is stored.

- *Sensor*: In case the tag has sensing capabilities.

2.1.3 Reader

The reader is the central part of the system, it controls all of the communication steps. The tag does not send any information if this is not first requested by the reader. It provides the tag with energy by generating a CW (continuous wave) and radiating it to the tag.

The Figure 2.1 shows the main parts of an UHF RFID reader :

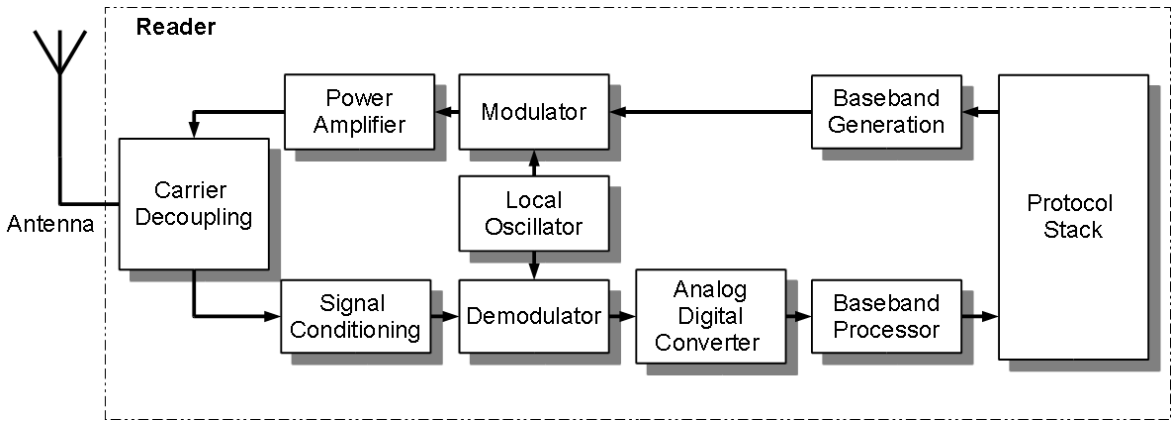

Figure 2.1: General UHF Reader Block Diagram

Protocol Stack

It is the state machine that is responsible for the communication protocol. The communication details are contained in here, the main activities are: to request data, inventory round, control the tag population and many others.

Transmitter

The transmitter consists of different parts:

- *Baseband Generation*: The information is channel-coded in order to create a baseband signal. This signal contains the information that is to be transmitted to the tag
- *Local Oscillator*: Is an electronic circuit used to generate a sinusoid signal that is used to generate the CW.
- *Modulator*: The baseband signal is used to modulate the CW signal which is later radiated and received by the tag(s).
- *Power Amplifier*: In order to be able to provide the tag with enough energy, the CW should have a certain power level. The power amplifier increases the power of the signal before it is fed to the antenna.
- *Antenna*: It is the radiating element of the system.

Figure 4.8, in section 4.3 shows a basic transmitter block digram.

Receiver

The receiver consists of different parts:

Carrier Decoupling: The reader can work in two different configurations:

Bistatic: This is the more natural way to decouple the carrier. The transmitter path and the receiver path are completely independent. Two antennas are used; one radiates the CW that provides the tag with energy. The second one is only used to receive the reflected wave of the tag. There is always a certain coupling between the to

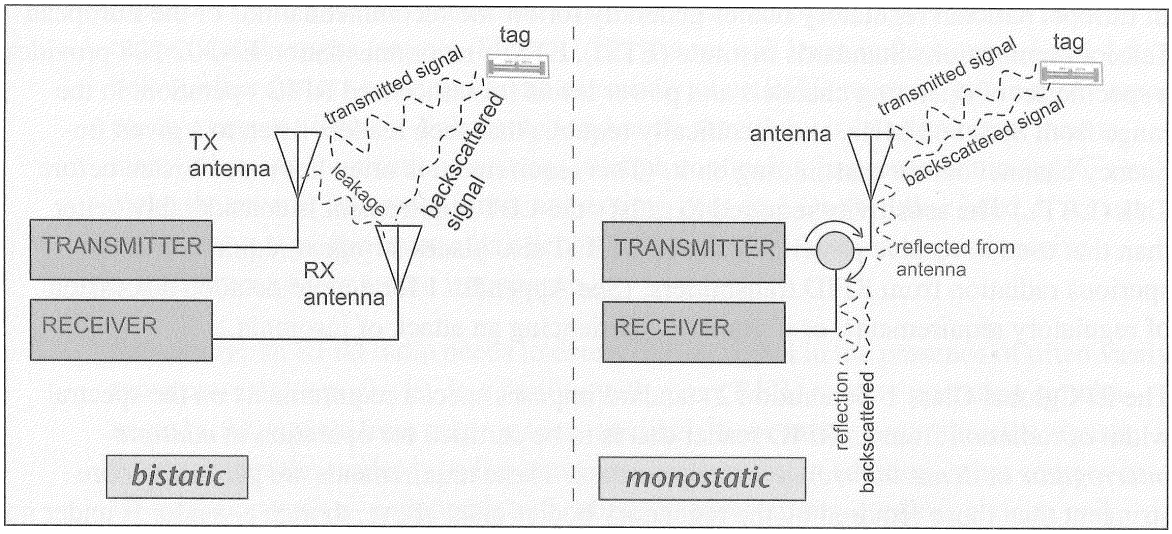

Figure 2.2: Bistatic and Monostatic Configuration [24]

antennas, the isolation between them is typically of 35 dB [29]. Figure 2.2 (left) shows a block diagram of the bistatic configuration.

This modus presents certain disadvantages:

- *Cost*: the cost of the reader is increased by the need of two antennas.
- *Installation*: the installation effort is increased as well, hence both antennas need to be correctly positioned. The position of the antennas and the reflections in the environment affect the carrier isolation.
- *Hand Held Devices*: the fact that two antennas are needed makes this configuration unsuitable for handheld devices.

Monostatic: Another possibility is to use only one antenna, this leaves the decoupling task to the electronic circuit and not to the physical positioning. The decoupling can be made by dedicated high frequency components, typically by a circulator. Figure 2.2 (right) shows the block diagram of a monostatic configuration. This is the typical mode used by UHF RFID readers. The achieved isolation is of 20 dB typically.

Signal Conditioning: This part includes any preprocessing the received signal requires: amplification, filtering, frequency shifting, etc.

Demodulator: The part of the receiver that separates the information signal from the high frequency carrier.

Baseband Processing: The information signal is coded in the baseband signal, but this one is influenced by the transmission channel and received together with noise. The algorithms that extract information out of the received signal are called baseband processing.

Typical Receiver Architecture

This work focus mainly on the receiver side, therefore the typical receiver architecture of an UHF RFID reader, working in a monostatic modus, is presented in this section. Figure 2.3 shows a basic functionality diagram of a standard reader.

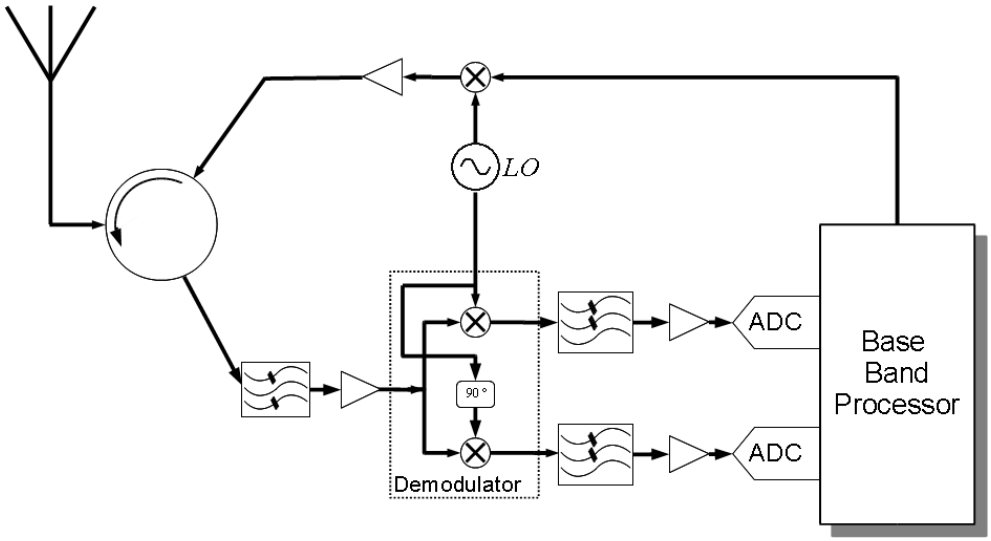

Figure 2.3: Typical Receiver Architecture of UHF RFID Readers [36]

The main components of a typical receiver are:

- *Carrier Decoupling*: It is typically made by using a simple circulator.
- *Signal Conditioning*:
  - The signal goes first through a band-pass filter in order to eliminate possible neighbor signals coming from other communication systems.
  - An amplification step is necessary since the power of the incoming signal is normally low.
- *Local Oscillator*: It is typically the same one used in the transmitter path, it can be used to demodulate the received signal as well.

- *Demodulator*: The radio architecture of the standard reader is a direct down converter or homodyne receiver. The received signal is directly multiplied by a signal of the same frequency as the carrier. This is a practical approach due that the carrier is generated in the reader, therefore an optimal signal for demodulation is directly available.

- *Baseband Processing*: The baseband is normally digitized leaving the baseband signal processing to the digital domain.

2.2 Backscatter Channel

The tag sends information back to the reader by means of the backscatter modulation technique. The tag changes the impedance matching circuit of the antenna in order to reflect the incoming wave. By modulating this reflected wave with the information signal it is possible to send a response back to the reader. Figure 2.4 shows an illustration of the backscatter principle.

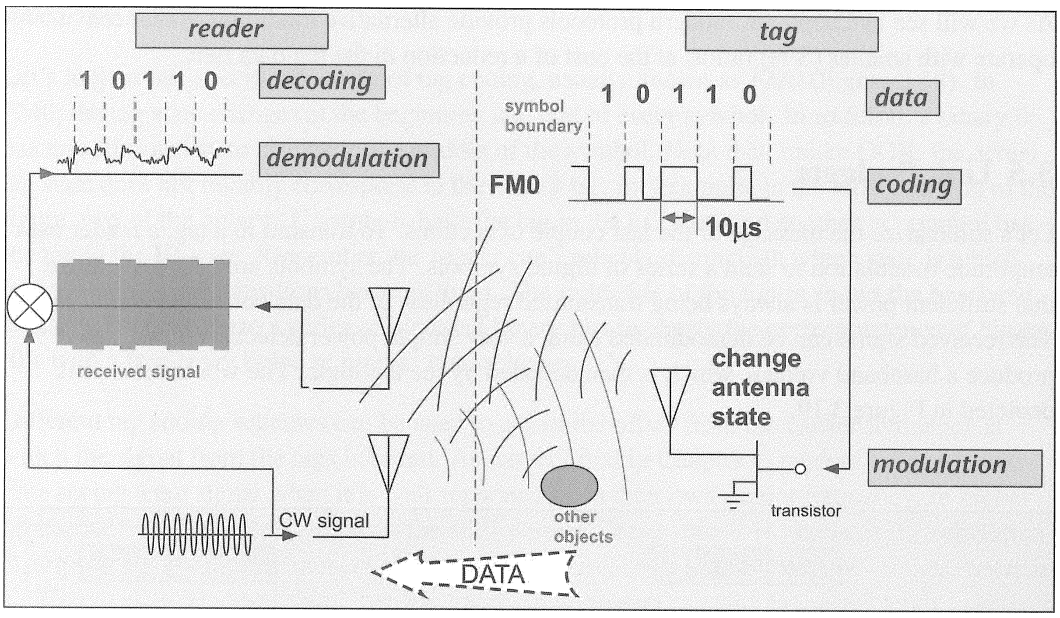

Figure 2.4: Backscatter Principle [24]

2.3 Digitization of Analog Signals

The first approach in improving the UHF RFID systems is to make most of the required signal processing in the digital domain, the question arises; where is the actual limit?, how close to the antenna could the signal be digitized?. The optimal solution for a digital processing approach is to have the signal in digital form as soon as possible, that is after the antenna. This is not practical for many reasons that would be explained in this section.

2.3.1 Challenges

Dynamic Range

According to the bandwidth of the antenna, other signals from neighbor channels could also be received. These signals could have greater power levels than the signal of interest. In other words, the power level of the *resulting* signal is increased and includes signals that not may be of interest. All these facts complicate the digital conversion. The ADC needs to have a big dynamic range in order to be able to digitize signals with small and high power levels at the same time. A pre-signal selecting step before the digital conversion is necessary.

Sample Rate

In the digital domain the signals can not be processed in a continuous form, they need to be sampled before they can be converted to a digital format. The fundamentals of signal sampling are basically described by the Nyquist-Shannon theorem [63] and [38]. This theorem says basically that a bandwidth limited continuous signal can be sampled and fully reconstructed, when the sampling frequency, further referred as f_s, has been chosen after:

$$f_s \geqq 2 \cdot (f_{max} - f_{min}) \tag{2.1}$$

By low-pass sampling, the f_{min} is considered to be 0, thus resulting in a sampling frequency after equation 2.1

$$f_s \geqq 2 \cdot f_{max} \tag{2.2}$$

In other words, a sampled signal can be reconstructed or represented if the sampling frequency is at least two times bigger than the maximal frequency component of the signal.

Aliasing: If there are any frequency components in the signal greater than the half of the sampling frequency, an image of this signal appears after the sampling. This is called an alias, and it is normally to be avoided, since it can distort the signal of interest. I.e. the digitized signal not longer corresponds to the original continuous signal. Although aliasing is a not desired effect, it is the basis of the under-sampling techniques. Nevertheless these techniques require a digital converting element with a wide bandwidth. An approach based on these techniques is presented in section 5.1.

Bandwidth

If the digital conversion is done directly after the antenna, the ADC needs to be able to convert the signals delivered by the antenna. Signals with frequencies higher than the bandwidth of the ADC are attenuated by the low-pass characteristic of the ADC input circuit.

2.3.2 Praxis

As it can be seen, all the limitations presented in section 2.3.1, apply mainly to the ADC. There are a few elements that are necessary in order to relax the requirements of the ADC.

Channel Selection

The signal delivered by the antenna can be filtered to select only the bandwidth of interest. Channel selection reduces the power level of the signal by eliminating the power contributions of the signals on neighbor channels, in this way the dynamic range of the signal is reduced.

Amplification

When the signal to be converted present low power level it is necessary to amplify it. If the power level is too small it may not be possible to digitize it. Amplification enables to use of the dynamic range of the ADC in an optimal way.

Frequency Conversion

There are electronic elements that enable the possibility of shifting a signal in frequency, these elements are called mixers. By converting the signal into a lower frequency domain it can be sampled at a slower rate thereafter.

2.3.3 Conclusion

The basic of UHF RFID systems and digitization have been presented in this chapter. It builds the foundations for the next chapters.

Chapter 3

Analysis of Signals in UHF RFID Systems

This chapter presents the characteristics of UHF RFID systems at signal level. First a mathematic modeling of the UHF RFID signals is given, followed by a simulation. The system model used in this section is shown in Figure 3.1.

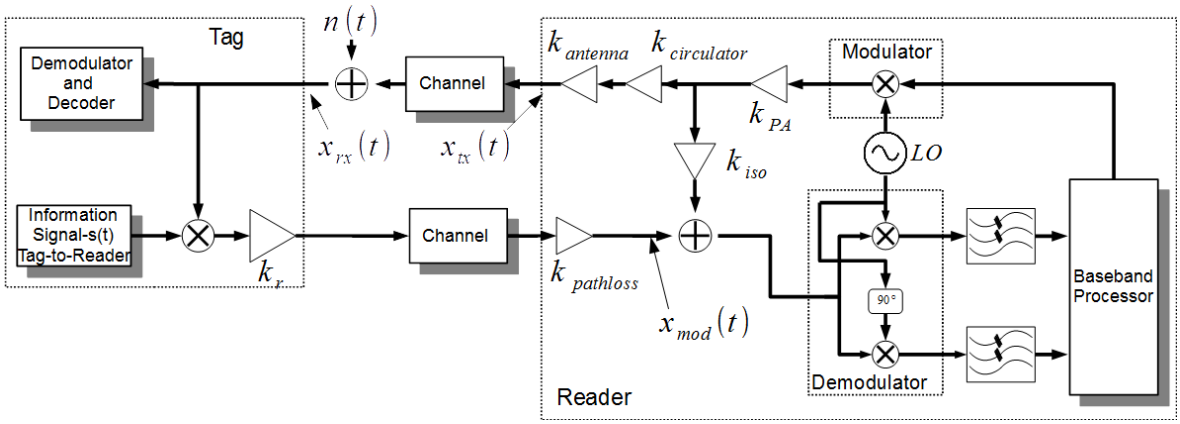

Figure 3.1: UHF RFID System Model

3.1 Mathematical System Description

The analysis begins with the local oscillator (LO), this element is used to generate the CW and a coherent demodulating signal for the demodulator. The LO can be

represented with

$$LO(t) = A_{LO} \cdot cos(2\pi \cdot f_{carrier} + \varphi_{LO}) \tag{3.1}$$

The PA amplification factor is represented by k_{PA}, the circulator loss by $k_{circulator}$ and the antenna gain by $k_{antenna}$. In this way the transmitted signal is represented as

$$x_{tx}(t) = k_{circulator} \cdot k_{antenna} \cdot k_{PA} \cdot A_{LO} \cdot cos(2\pi \cdot f_{carrier} + \varphi_{LO}) \tag{3.2}$$

the signal received at the tag is (without considering the multipath effect)

$$x_{rx}(t) = k_{PathLoss} \cdot A_{tx} \cdot cos(2\pi \cdot f_{carrier} + \varphi_{LO}) + n_0(t) \tag{3.3}$$

where $n_0(t)$ is Gaussian noise, $A_{tx} = k_{circulator} \cdot k_{antenna} \cdot k_{PA} \cdot A_{LO}$ and the path loss $k_{PathLoss}$ factor is determined by the sum of the line-of-sight and several single reflections at the tag's position [57]. And is given by

$$k_{PathLoss} = (\frac{\lambda}{4})^2 \cdot |1 + \sum_{n=0}^{N} \Gamma_n \frac{d}{d_n} e^{-jk(d_n - d)}|^2 \tag{3.4}$$

where d is the distance of the direct ray path, Γ_n the reflection coefficient of the n^{th} reflected ray path and $\frac{d}{d_n} e^{-jk(dn-d)}$ is the addition of the reflected rays. This addition can be constructive or destructive according to phase difference. The backscattered or modulated signal is given by

$$x_{mod}(t) = k_r \cdot A_{rx}[s(t)] \cdot cos(2\pi \cdot f_{carrier} + \varphi_{mod}[s(t)]) + n_0(t) \tag{3.5}$$

where k_r is the reflexion coefficient of the tag, i.e. how much of the incoming power is used/reflected to create a backscatter signal. Here $A_{rx} = A_{tx} \cdot k_{PathLoss}$ and $s(t)$ denotes the tag's binary data sequence of 1s and 0s. The multiplication with A_{rx} represents the ASK modulation part and the $\varphi_{mod}[s(t)]$ the phase modulation part. The received signal at the input of the demodulator is

$$\begin{aligned} x_{received}(t) = {} & k_d \cdot A_{mod}[s(t)] \cdot cos(2\pi \cdot f_{carrier} + \varphi_{mod}[s(t)]) \\ & + k_d \cdot k_{iso} \cdot k_{PA} \cdot A_{LO} \cdot cos(2\pi \cdot f_{carrier} + \varphi_{LO2}) + n_0(t) \end{aligned} \tag{3.6}$$

where $A_{mod} = k_r \cdot A_{rx}$, the isolation factor of the carrier decoupling element is represented by k_{iso} and φ_{LO2} is the phase of the coupled carrier. k_d denotes the transfer

coefficient of the receiver taking into consideration the total loss or gain of the RF bandpass filters, the power splitter and amplifiers. The demodulator is a coherent I-Q demodulator, the received signal is multiplied by LO signal for the I path and by LO shifted 90° for the Q path. A lowpass filter eliminates the second harmonic elements that result from the multiplication, these are not presented for simplicity. The first element in equation 3.6 is the demodulation of the backscatter signal, i.e. the baseband that contains the information transmitted by the tag. The second part is the demodulation of the coupled carrier which leaks into the receiver path. Finally the demodulator output can be expressed as

$$\begin{aligned} x_I(t) = k_d \cdot A_{mod}[s(t)] \cdot cos(\varphi_{mod}[s(t)] - \varphi_{LO}) \\ + k_d \cdot k_{iso} \cdot k_{PA} \cdot A_{LO} \cdot cos(\varphi_{LO2} - \varphi_{LO}) + n_0(t) \end{aligned} \tag{3.7}$$

for the in-phase channel [28]. It is important to mention that the frequency of the LO and the received signal have the same frequency but not the same phase. The difference between φ_{LO2} and φ_{LO} results in a DC (Direct Current) level determined mainly by

$$cos(\varphi_{LO2} - \varphi_{LO}) \tag{3.8}$$

The difference between φ_{mod} and φ_{LO} manifests as a DC level determined mainly by

$$cos(\varphi_{mod}[s(t)] - \varphi_{LO}) \tag{3.9}$$

as well.

The quadrature channel can be expressed as

$$\begin{aligned} x_Q(t) = k_d \cdot A_{mod}[s(t)] \cdot sin(\varphi_{mod}[s(t)] - \varphi_{LO}) \\ + k_d \cdot k_{iso} \cdot k_{PA} \cdot A_{LO} \cdot sin(\varphi_{LO2} - \varphi_{LO}) + n_0(t) \end{aligned} \tag{3.10}$$

in the same way the phase difference between φ_{LO2} and φ_{LO} results in a DC level determined mainly by

$$sin(\varphi_{LO2}[s(t)] - \varphi_{LO}) \tag{3.11}$$

and the phase difference between φ_{mod} and φ_{LO} results in a DC level determined mainly by

$$sin(\varphi_{mod} - \varphi_{LO}) \tag{3.12}$$

as well.

3.1.1 Analysis

After representing the signals mathematically some characteristics of UHF RFID systems can be seen.

Demodulator

The coherent demodulation of the received signal has some unique characteristics in UHF RFID systems.

- The received signal is the sum of the modulated backscatter, a clutter backscatter signals coming from reflective objects in the operating environment and the carrier leakage.
- Due to the high level of the leakage signal in relation to the modulated backscatter, it is hardly possible to synchronize the demodulating signal (LO) with the phase of the modulated backscatter. In other words the I-Q demodulator tracks mainly the phase of the leaked carrier signal (see equations 3.8 and 3.11).
- Since the level of the leakage signal is bigger than the level of the modulated backscatter, the resulting DC level is mainly determined by the difference between φ_{LO2} and φ_{LO}. In other words the I and Q paths can not be combined directly, neither phase nor magnitude can be obtained directly out of the I-Q complex representation.

Phase Noise

In real coherent receiver architectures the phase noise of the demodulating signal creates a time-dependent phase difference between the phase of the incoming signal and the phase of the demodulating signal. This difference is transformed into a time-dependent DC level and finally into amplitude noise. This noise source is of big important in UHF

RFID systems since it influences the small baseband signal greatly. See equations 3.13 and 3.14, $A_{bs} = k_d \cdot A_{mod}$ and $A_{leakage} = k_d \cdot k_{iso} \cdot k_{PA} \cdot A_{LO}$.

$$\begin{aligned} x_I(t) = A_{bs}[s(t)] \cdot cos(\varphi_{mod}[s(t)] - (\varphi_{LO} + \varphi_n(t))) \\ + A_{leakage} \cdot cos(\varphi_{LO2} - (\varphi_{LO} + \varphi_n(t))) + n_0(t) \end{aligned} \tag{3.13}$$

$$\begin{aligned} x_Q(t) = A_{bs}[s(t)] \cdot sin(\varphi_{mod}[s(t)] - (\varphi_{LO} + \varphi_n(t))) \\ + A_{leakage} \cdot sin(\varphi_{LO2} - (\varphi_{LO} + \varphi_n(t))) + n_0(t) \end{aligned} \tag{3.14}$$

where $\varphi_n(t)$ represents the phase noise.

Multipath and Fading

From equations 3.3 and 3.4 can be seen that the multipath effect affects mostly the energy level at the tag. If the energy level drops below the tag's requirement the tag will simply not be able to function.

If the channel response is time-variant, fading is created hence equation 3.3 is now 3.15

$$x_{rx}(t) = k_{PathLoss}(t) \cdot A_{tx} \cdot cos(2\pi f_{carrier} + \varphi_{LO}) + n_0(t) \tag{3.15}$$

I.e. the energy level at the tag is time-variant as well. Fading not only may affect the energy available for the tag but the baseband signal at the receiver as well. With the energy level at the tag changing, variating baseband amplitudes can be seen at the receiver side (fading). Fading can create ISI (Inter-Symbol-Interference). Some field test and experiments have been made in [57], [54], [60], [14].

3.2 Simulation

A system simulation is presented in order to get a better overview of the signal characteristics in UHF RFID. The simulation model is shown in Figure 3.2. The simulation was made using Matlab™ [2]. It is important to notice that the simulation was done trying to keep all parameters as close to reality as possible. Nevertheless many real-environment influences are hard to simulate. All the spectra presented in this section where calculated by using a FFT with Hanning window. The parameters for the simulation are:

- *Carrier Frequency (f_c)*: 866.5 MHz
- *Transmission Power (P_T)*: 20 dBm
- *Reader Antenna Gain ($k_{antenna}$)*: 9 dB (typical for patch antennas used in RFID)
- *Tag Antenna Gain*: 0.7 dB
- *Carrier Isolation k_{iso}*: 20 dB (typical nominal value of standard circulators)

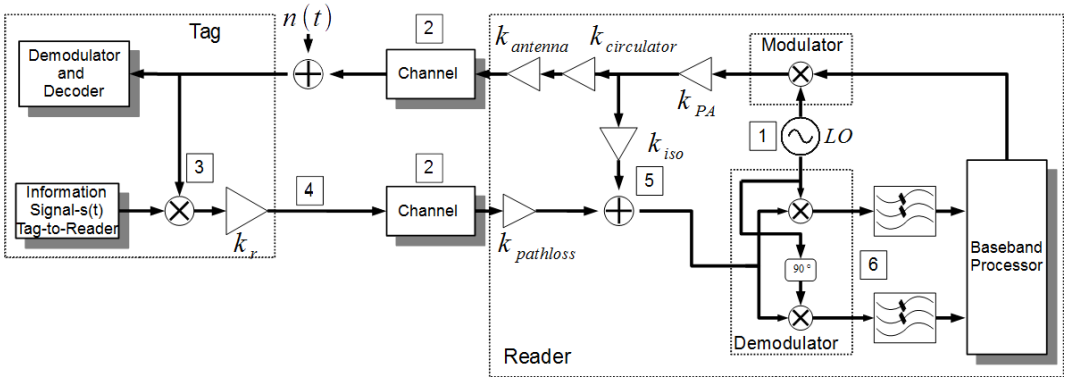

Figure 3.2: UHF RFID Simulation Model

3.2.1 Carrier

Marker-1. The carrier is a sinusoid signal with a frequency of 866.5 MHz which is the center of the European 865 MHz SRD (Short Range Devices) band. Figure 3.3 shows the time signal in the top plot and the frequency domain in the bottom plot, the side lobs are caused by the FFT window. The PA and the antenna gains are already considered, the power of the carrier is 29 dBm (approx. 1 Watt).

3.2.2 Channel

Marker-2. The channel is considered to be static. Other 10 reflections are included whose magnitudes and delays are Rayleigh distributed. The distance between reader and tag d is set to 6 meters with a direct-line-of-sight. Figure 3.4 shows the channel impulse response on the top of the plot and the frequency response on the bottom plot. The free path loss is already considered in the channel response.

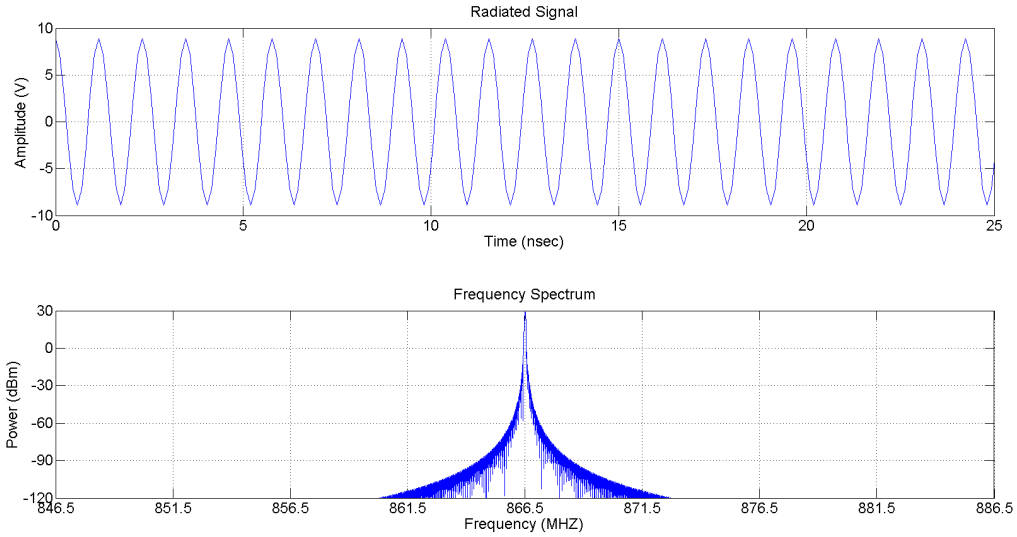

Figure 3.3: Carrier Signal in Time and Frequency Domain

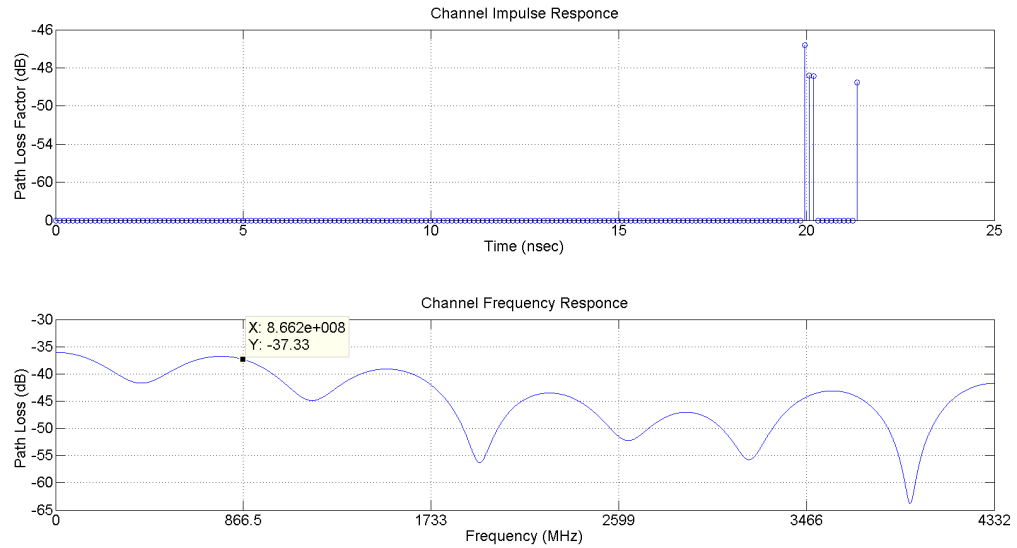

Figure 3.4: Channel Impulse response

From the top plot can be appreciated how the first ray takes approx. 20 *ns* to travel to the tag, the magnitude of the impulse is the path loss the ray suffers while traveling to the tag. The other impulses represent the reflections arriving after. Each reflection contributes to the final signal level at the tag. This can be better seen at the frequency response, the path loss suffered by the 866.5 MHz wave is of approx. -37 dB, instead of the calculated -45.9 dB for a single path. The reflections can increase or decrease the final amplitude of the signal, depends on how the signals add each other. In Figure 3.5 can be seen how the carrier is attenuated approx. -37 dB. See Figure 3.4.

3.2.3 Signal at the Tag

Marker-3. After the signal has been passed through the channel some white noise is added. In Figure 3.5 it can be seen how the time signal in the top plot is been changed by the noise. The bottom plot shows the frequency spectrum of the signal at the tag. The amplitude of the carrier has been attenuated by the channel, the influence of the channel's frequency response can be seen in the frequency spectrum of the signal at the tag.

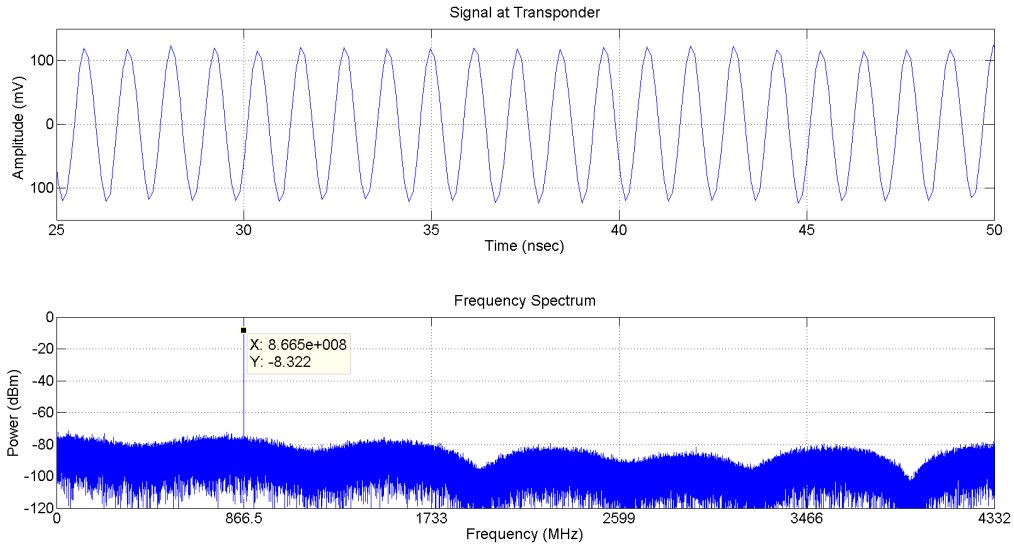

Figure 3.5: Signal at the Transponder

3.2.4 Backscattered Signal

Marker-4. The incoming signal at the tag is PSK modulated with a phase hop of 25° and a reflection factor of 6 dB (25%) (k_r) which are a typical values for UHF tags [24]. The Figure 3.6 shows the modulated backscatter after is has traveled back to the reader. On the top plot is the time signal; the modulation can not be easily seen in time but in frequency domain. The side lobes around the carrier are the frequency components of the baseband signal. The signal used to modulate is a series of FM0 random symbols. The result is a carrier-less modulation, i.e. most of the energy is distributed on the side lobs.

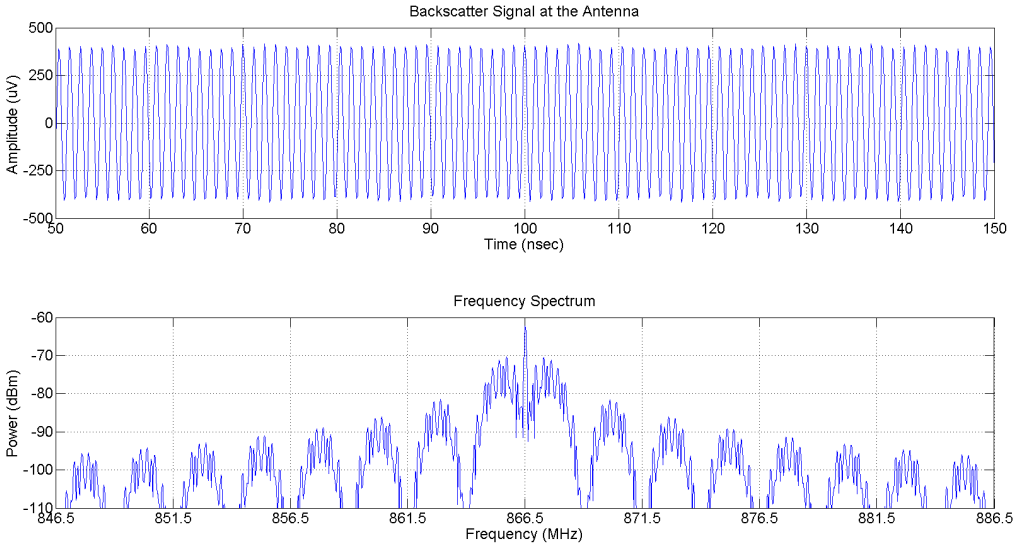

Figure 3.6: Modulated Backscatter

3.2.5 Carrier Leakage

Marker-5. When the signal arrives at the reader, some part of the original carrier overlaps with the modulated backscatter signal. The backscatter is in this case phase modulated and added to the carrier results in amplitude modulation. This effect can be seen in Figure 3.7 on the top plot. The bottom plot shows the frequency spectrum of the signal at the input of the demodulator. It can be clearly seen how the carrier has a quite higher power level than the backscattered signal, approx. 66 dB difference between the carrier and the first side lobe in this case.

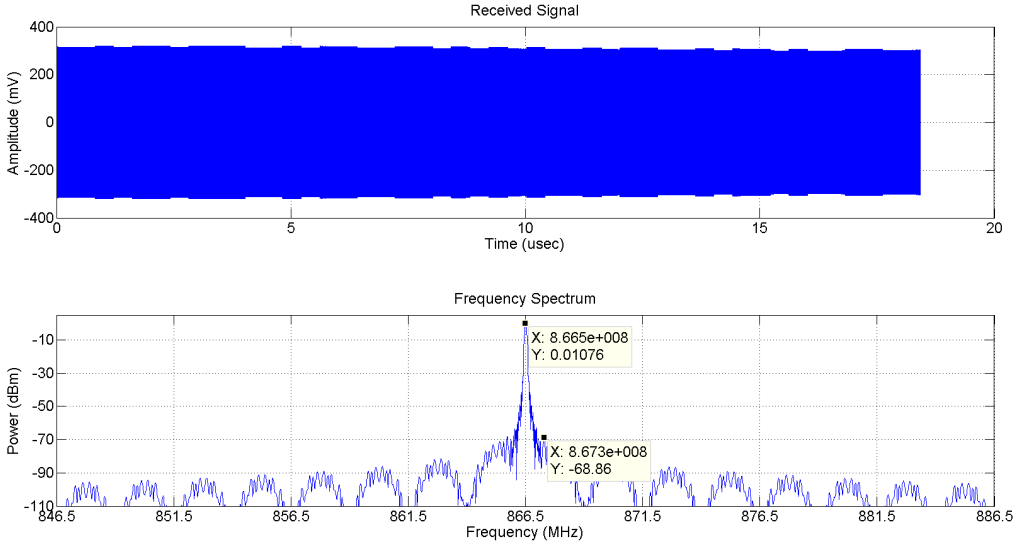

Figure 3.7: Demodulator Input

3.2.6 Demodulation

Marker-6. After the I-Q demodulator and the lowpass filter, the baseband signal that was used to modulate the backscatter is obtained. The plots on the left side of the Figure 3.8 are the signals in time domain.

It can be seen how a relative high DC level is added to the baseband signal, this offset depends mainly on the carrier's leakage and a small part on the phase difference between the modulated backscatter and the demodulator's local oscillator. The plots in the right side of Figure 3.8 show the frequency spectrum of each paths.

The simulation section has covered the UHF RFID system all the way from the transmitter to the receiver paths. Signal after the demodulator is called baseband signal and contains the information transmitted by the tag, nevertheless the signal contains noise and it may be distorted during the transmission. The next step in the system is the baseband processor.

3.3 Baseband Processing

The goal of the baseband processing is to recover the information out of the baseband signal. The required algorithms depend on the characteristics of the baseband signal. The information signal has been exposed to noise and disturbances during the

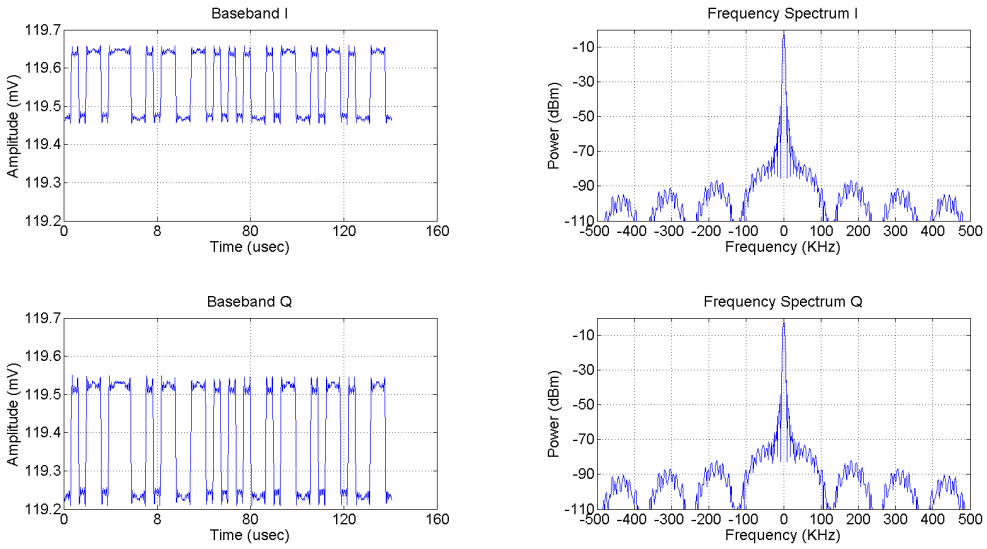

Figure 3.8: Demodulator Output: In-phase and Quadrature paths with corresponding frequency spectrum

transmission process. The main characteristic to be considered in UHF RFID are:

- *Data Rate*: How fast are the symbols sent. Higher data rate are more susceptible to the channel conditions than lower data rates.

- *Signal-to-Noise-Ratio*: It is the ratio between the signal power and the noise power. It its normally given in dB, the higher the ratio the easier it is to recover the information signal.

- *Line Coding*: The information signal is encoded before it is transmitted, this is called line coding. In UHF RFID the information is line-coded with the FM0 and Miller coding scheme.

- *Distortion*: The symbol form may be changed during the transmission. This can cause ISI and may require an equalization process before the signal can be decoded.

- *Carrier-to-Signal-Ratio*: The high carrier leakage complicates the recovery of the information signal. It is measured in dBc (dB to carrier)

3.3.1 Line Coding in UHF RFID

This work refers mainly to the EPCglobal Class 1 Gen 2 standard and the system specification given in it [27]. According to this standard the tag-to-reader communication takes place using backscatting modulation techniques. In other words the tag uses the electromagnetic field, provided by the reader, to transmit the information back to the reader and to power itself. The information is encoded in 4 possible forms FM0, Miller 2, Miller 4 or Miller 8 (see Figure 3.10).

The reader requests the information from the tag and specifies the data rate as well as the coding scheme to be used. There are some characteristics referring to this coding scheme: the FM0 coding is the base for the other three types. The Miller 2 to Miller 8 can be seen as a combination of FM0 symbols. The auto and cross correlation functions of the FM0 and Miller symbols show some special characteristics.

FM0 symbols

- The 2 FM0 symbol forms are orthogonal to each other. The auto correlation function shows a dominating peak at the center of the function (symbol period). The cross correlation function is relative flat and shows no peak at the center of the correlation output. See Figure 3.9.

- In a sequence of FM0 encoded data, the phase of the signal is changed with every symbol representing a 0; however, this does not affect the synchronization of the sequence, i.e. the symbol form can not be misinterpreted by the decoder if the sequence is shifted in time.

Miller symbols

- The Miller symbols are basically constructed out of FM0 symbols.

- The difference between Miller 2, 4 and 8 is just the length of the symbols.

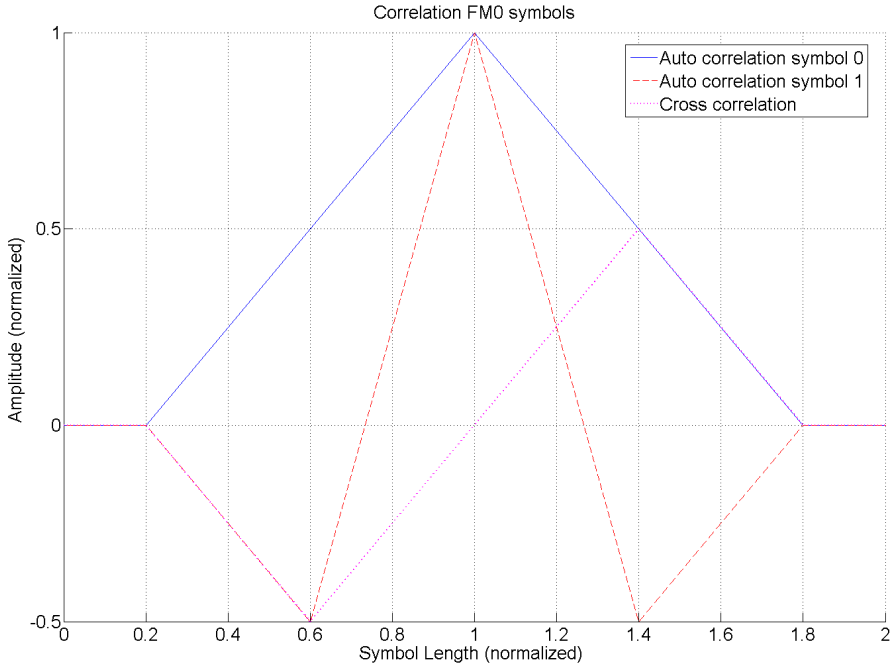

Figure 3.9: Auto and Cross Correlation Functions of the FM0 Symbols

- The symbol structure is mainly an equal-spaced level toggling during the symbol length. For representing a 1 the toggling phase is changed at the middle of the symbol length.
- The Miller symbols are not fully orthogonal to each other. The auto correlation functions show a dominant peak at the center of the function (symbol period) but surrounded by other peaks on both sides. The cross correlation function is zero only at the center for the correlation output. See Figure 3.11.

The concept of these long symbols representing a single one or zero is not optimal. Another coding scheme can be used, one that takes advantage of orthogonality and the correlation gain.

3.3.2 Typical Baseband Processing

There are many ways to recovery the information signal, nevertheless most of them are based on the correlation or matched filter principle. Basically the symbol form of the information signal is known to the receiver. This one correlates the received signal with a copy of the symbol forms, the output of the correlation gives the likelihood

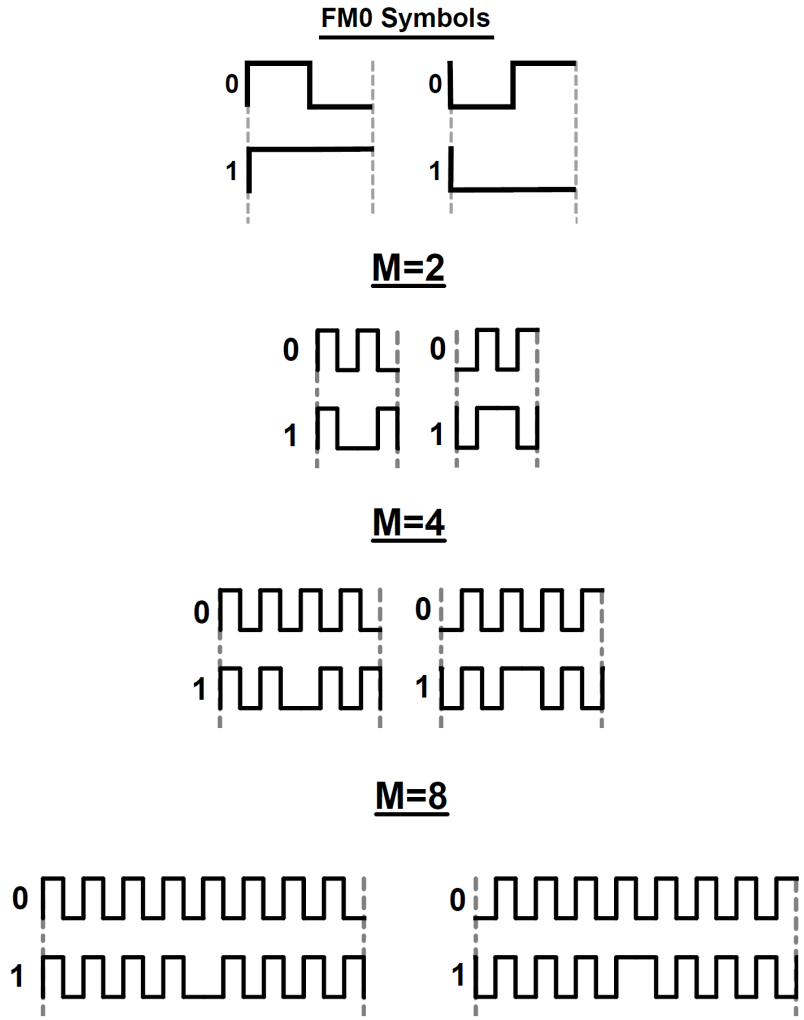

Figure 3.10: Channel Coding Scheme for Tag to Reader Communication as Specified in EPCglobal Class 1 Gen 2 [27]

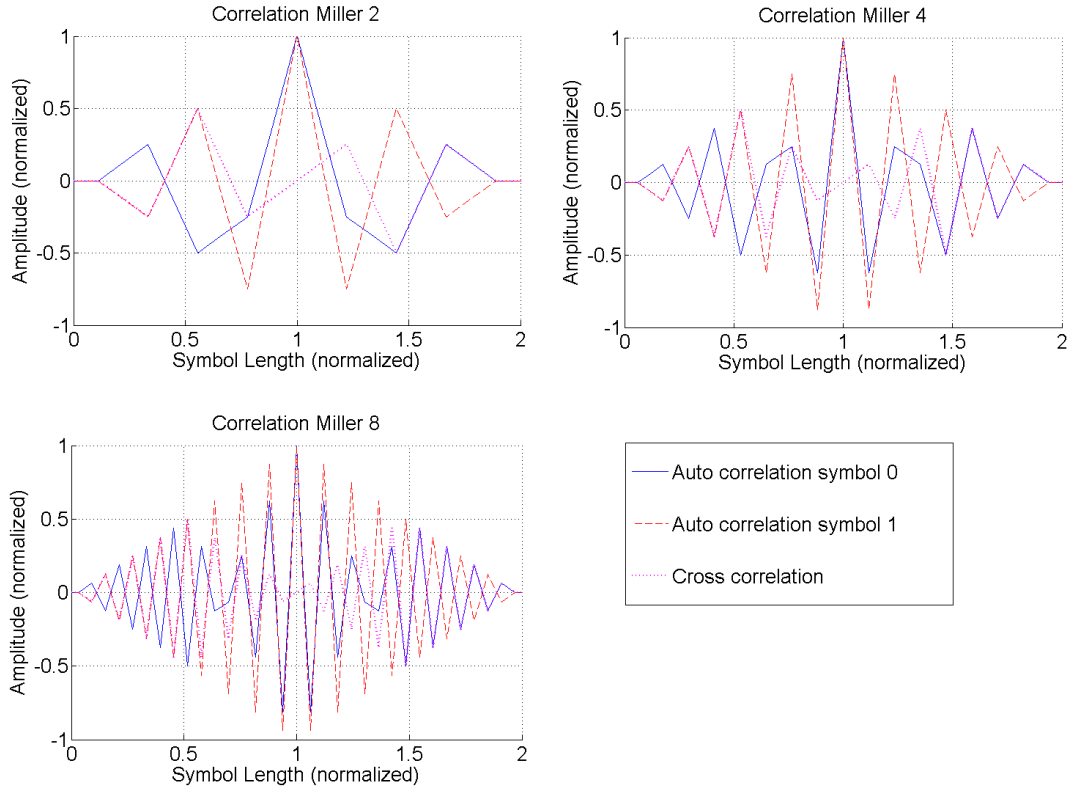

Figure 3.11: Auto and Cross Correlation Functions of the Miller symbols

of the received signal and the known symbol. This method is know as ML-receiver (Maximum-Likelihood).

The actual baseband processing algorithms of state-of-the-art readers is not public, nevertheless there are some publications which present some baseband processing approaches. In [12] the received signal is integrated with half of the symbol period, in this way each high or low level of the encoded signal is recognized, the integrated signal is passed through a comparator in order to decide whether a high or a low level was received (see Figure 3.12).

In [65] a symbol correlator with a length of 3/2 of a symbol is proposed, this brings a 3 dB improvement on the BER (Bit-Error-Rate) compared to the correlator with a length of 1 symbol period. The algorithm is presented using the FM0 symbols, nevertheless it can be extended to the Miller symbols due to the fact that these symbols can be separate in single FM0 symbols (see Figure 3.13).

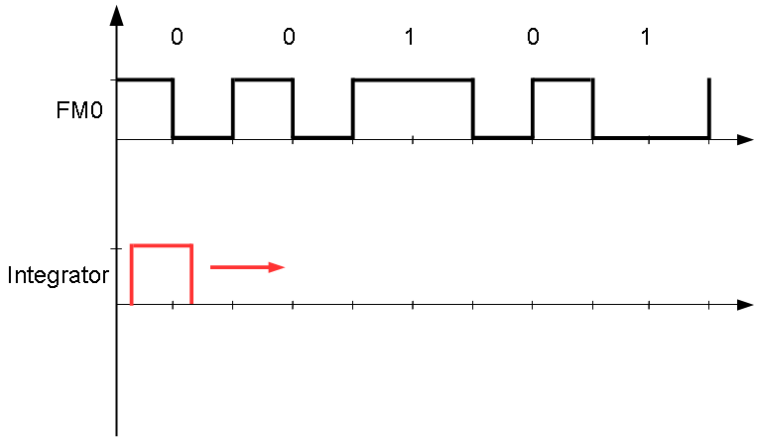

Figure 3.12: Half Symbol Integrator

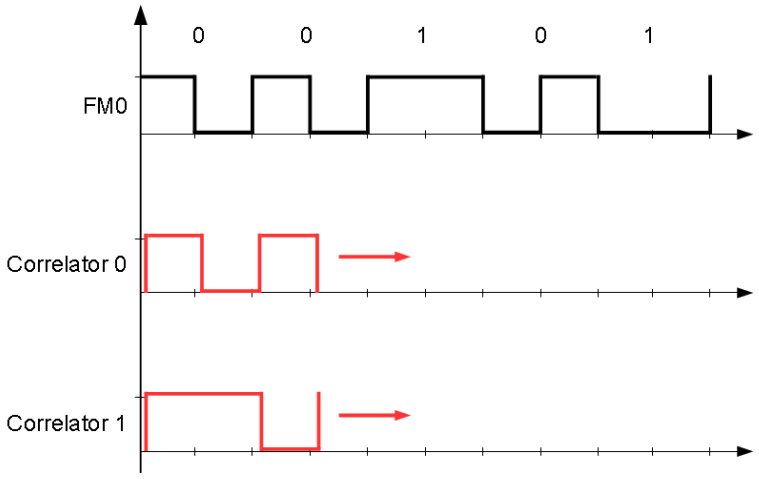

Figure 3.13: 3/2 length Symbol Correlator

Another practical correlator can be built by using the FM0 symbols. For the Miller encoded signals the symbol form is separated in its single FM0 symbols and can be reconstructed back to the original coding in a further processing step.

3.4 Conclusion

This chapter presented a basic analysis and a simulation of the signals in UHF RFID systems. It builds the bases for the following chapters where the system optimizations and improvements are presented.

Chapter 4

Test and Prototyping Platform

In order to be able to test and implement new algorithms a test platform is needed. This platform should have following characteristics:

- *Modular construction*: the main components of the platform should be modular. In this way different approaches can be followed by just changing or interconnecting modules.
- *Flexible*: the platform should provide a variety of resources for signal processing.
- *Re-programmable*: the platform should be reusable by simple means.
- *High performance*: as part of the flexibility, the resources of the platform should not present a close limitation on the algorithm development.
- *Short time-to-prototype*: the complexity of stepping the test platform to a possible prototype should be kept at minimum.

4.1 Description

There is not an out-of-box product that satisfy all the requirements given. Therefore a platform was developed and constructed out of different existing elements. Figure 4.1 presents an overview of the main components of the test platform.

The PC controls and configures the FPGA, this one controls the transmitter and the receiver. The last two are connected to the antenna by means of a carrier decoupling element.

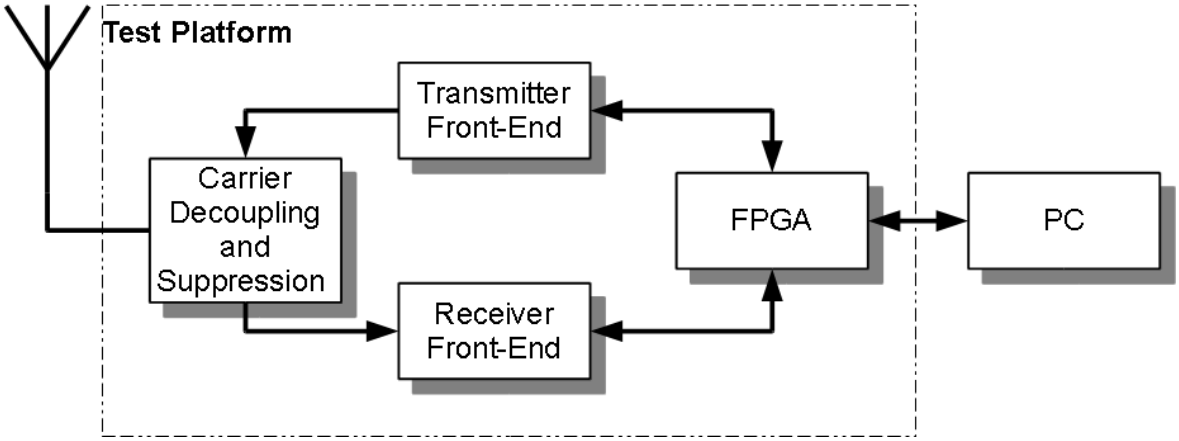

Figure 4.1: Overview of the Test Platform

4.2 Receiver

The receiver is the part of most interest in this work, for the main challenge of an UHF RFID reader consist in recovering the information data sent by the tag. The communication reader-to-tag is relatively simple. Figure 4.2 shows the block diagram of the test platform's receiver.

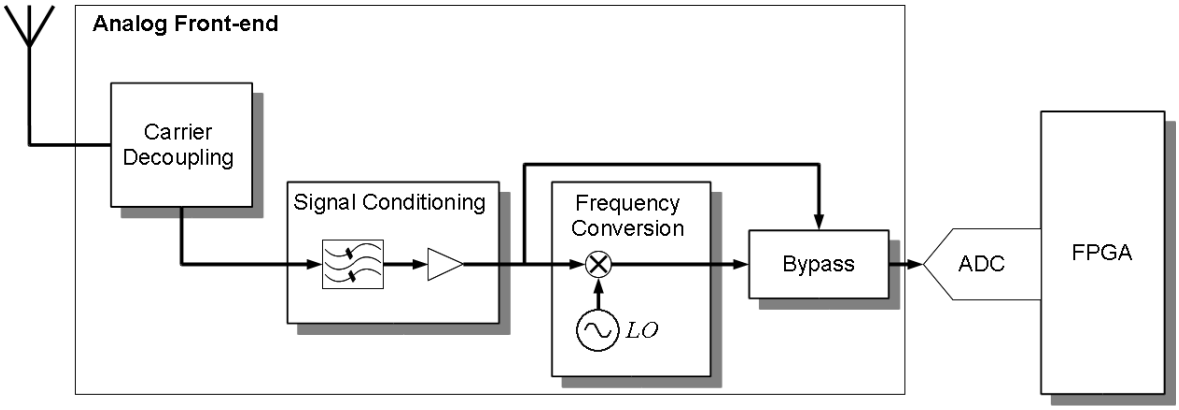

Figure 4.2: Block Diagram of the Receiver

4.2.1 Analog Front-End

The analog front-end prepares the signal before the analog to digital conversion. The main tasks are:

- Carrier Decoupling and Suppression

- Amplification
- Frequency Conversion (if required)

Carrier Decoupling and Suppression

There are some carrier decoupling modules that can be used with the test platform. This modules can be used to configure the platform either in monostatic or bistatic modus.

Bistatic: For the bistatic configuration is basically just a second antenna necessary. No special module is needed.

Monostatic: For the monostatic configuration there are three different possibilities:

- **Single Circulator.** Is the simplest carrier decoupling module, there is just a single circulator configured to work in standard from. Figure 4.3 shows a photograph of the single circulator module.

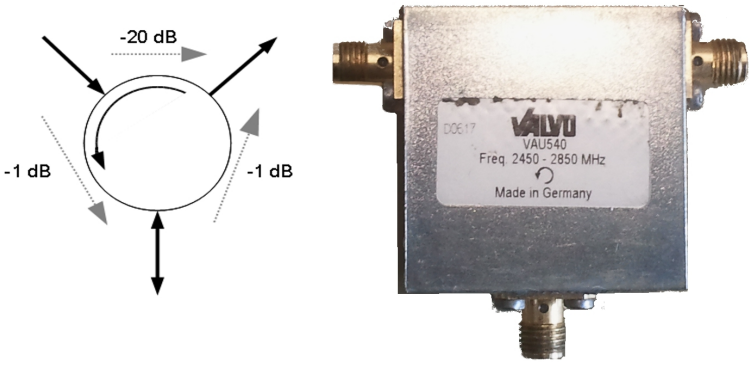

Figure 4.3: Single Circulator Module

- **Double Ciruculator.** There is a second module that uses 2 circulators working together to increase the isolation. The function details are of not interest in this work but can be found in [61]. Figure 4.4 shows a photograph of the double circulator module.

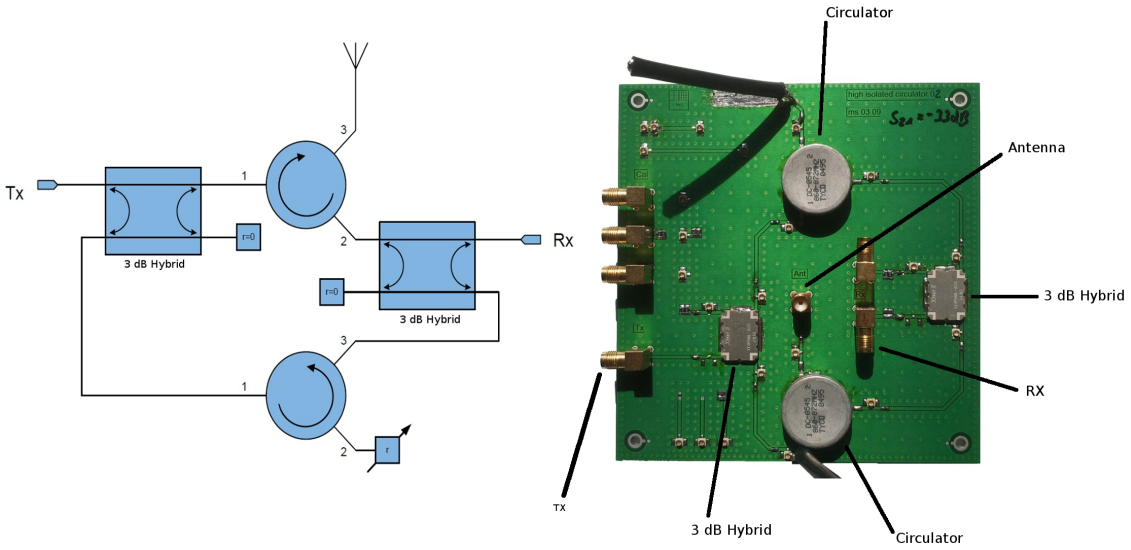

Figure 4.4: Double Circulator Module [61]

- **Active Carrier Decoupler.** Another way to increase the carrier isolation is by actively add an extra signal in the receiver in order to eliminate the carrier. This third module would be presented in detail in chapter 6.

Signal Conditioning

There is a variety of IC modules that can be used to amplify and filter the signals.

Frequency Conversion

There is a frequency shift module that can be integrated in the receiver path in order to shift the signal to a lower frequency. This frequency is called IF (Intermediate Frequency). The required sample rate is reduced in this case. The frequency conversion module can be bypassed.

4.2.2 Analog Digital Converter

To add flexibility to the system, most of the signal processing should take place in the digital domain. Therefore an analog to digital converter (ADC) works as interface between the analog signal processing and the digital signal processing. There are mainly two ADC modules that can be used on the test platform, their use depends on the desired system configuration.

12 bits @ 500 MSPS

One of the ADC modules can sample signals up to 500 MSPS (Mega Samples Per Second) and has a resolution of 12 bits. The low resolution of this ADC module could be of a disadvantage when sampling signals with a high dynamic range, but at the same time it allows to sample signals with high frequency components. It also has a relative high bandwidth which makes it suitable for sampling RF signals directly using under-sampling techniques. Figure 4.5 shows a photograph of the ADC module.

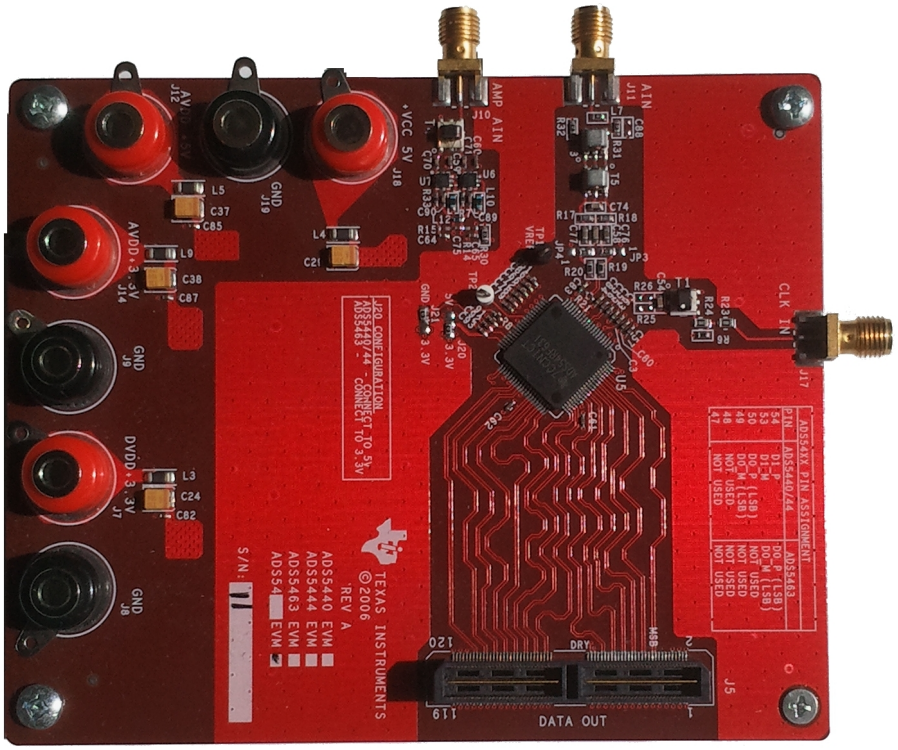

Figure 4.5: 12-bits ADC [3]

16 bits @ 105 MSPS

The second ADC module has a bigger dynamic range (higher resolution). It is suitable for sampling signals with small power levels and lower frequency components. Figure 4.6 shows a photograph of the ADC module.

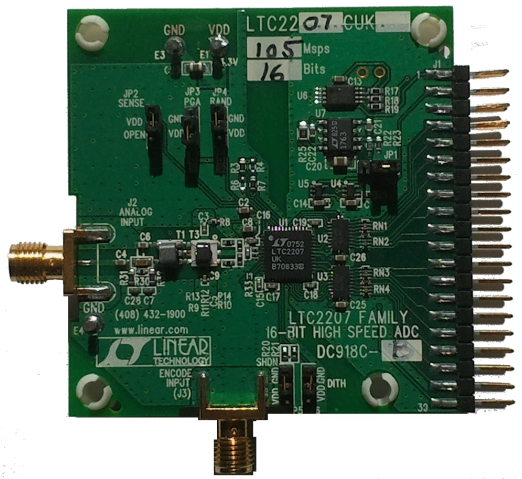

Figure 4.6: 16-bits ADC [1]

4.2.3 Signal Processor

The main element of the test platform is the signal processor. The signal processing is done in the digital domain, this adds flexibility to the system. The processing algorithms are defined in software, i.e. the signal processor can realize different tasks by just changing the running program. This reduces the time cost for test and implementation. These kind of systems are called *Rapid Prototyping Platforms*.

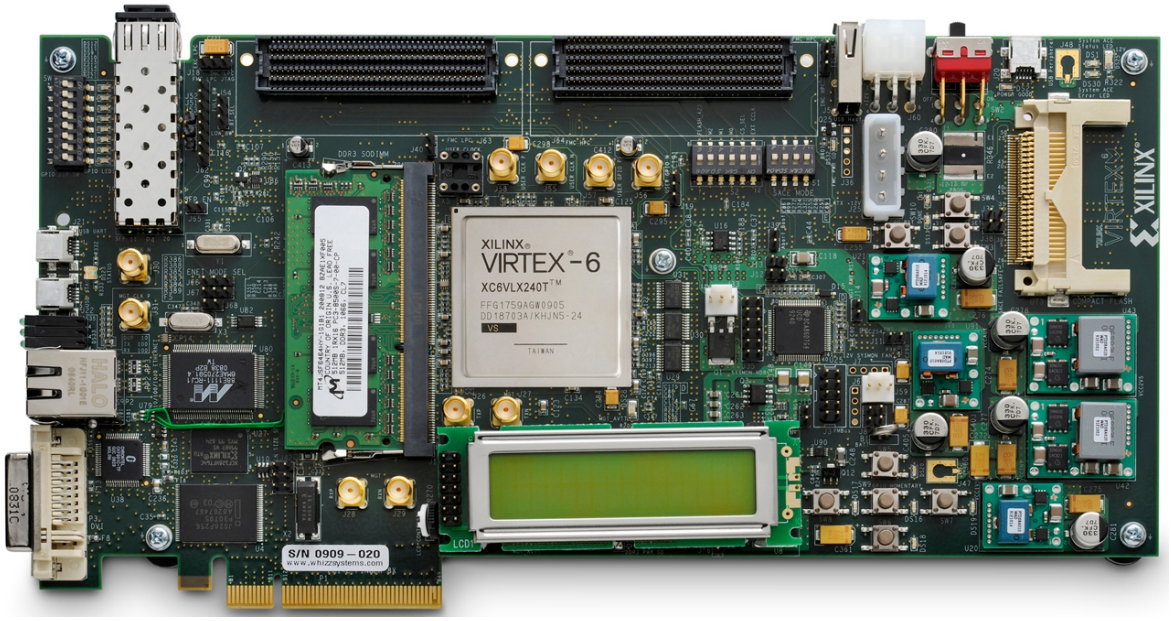

Figure 4.7: Virtex^{TM} 6 Evaluation Board [4]

FPGA

The signal processor chosen for the test platform is an FPGA (Field Programmable Gate Array). FPGAs are programmable logic components that can be configured to work as any digital circuit. Different elements can be programmed to work in parallel, this makes them a feasible way to defined radio elements (demodulators, filters etc.) in software. Figure 4.7 shows a photograph of the FPGA development board.

4.3 Transmitter

For the transmitter path a single module was developed. In this module just the basic functions are implemented, since the transmitter is not the main focus in this work. Figure 4.8 shows a block diagram of the transmitter.

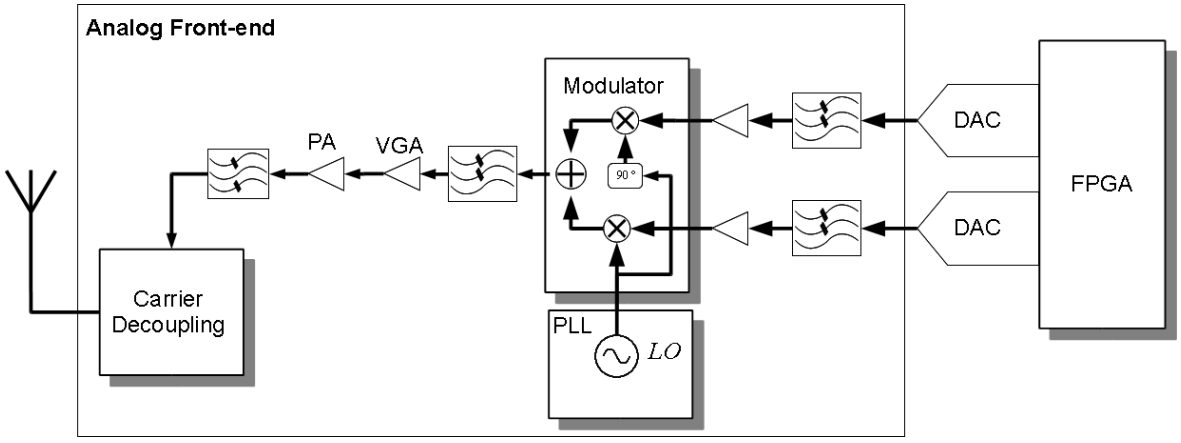

Figure 4.8: Block Diagram of the Transmitter

4.3.1 Baseband Generator

The baseband generation takes place in the FPGA. Here the digital signal is channel coded and passed through a symbol former. The baseband generator delivers two signals: In-phase and Quadrature (I and Q). In this way different modulation schemes are supported.

4.3.2 Digital Analog Conversion

The first element in the analog front-end is the digital analog converters (DAC). These components convert digital signals into analog signals. The DACs in the transmitter module have 14 bits resolution and can convert signals at 125 MSPS maximum. Figure 4.8 shows the DACs as interface between the FPGA and analog front-end.

4.3.3 Lowpass Filter

After the DAC it is necessary to have a lowpass filter, this eliminates the signal images resulting from the sampling process. The filtering is done by an integrated differential op-amp (operation amplifier), the op-amp has an embedded 4^{th} order lowpass filter and can be used for amplification when needed. (See Figure 4.8).

4.3.4 I-Q Modulator

According to the EPCGlobal Class 1 Gen2 standard [27], the supported modulation types for the reader-to-tag communication are: DSB-ASK (Double Side Band- Amplitude Shift Key), SSB-ASK (Single Side Band- Amplitude Shift Key) and PR-ASK (Phase Reversal- Amplitude Shift Key) [27]. In order to generate this modulation schemes, an I-Q (In phase-Quadrature) modulator is necessary. (See Figure 4.8).

Filter

The lowpass filter after the modulator eliminates harmonic elements resulting from the multiplication process.

4.3.5 PLL

The transmitter includes a PLL that is used as frequency synthesizer. It can generate sinusoid signals from 860 MHz to 960 MHz and can be configured through a digital interface. This element creates the CW that is transmitted to the tag .

4.3.6 Power Block

The signal power after the antenna should be strong enough to provide the tag with energy. The allowed transmission power in the SDR band is 2 Watts or 33 dBm (decibel

milliwatt) of ERP (Effective Radiated Power). This requires an amplification section strong enough to provide the required power. The power block consist of two parts:

Variable Gain Amplifier

The variable gain amplifier or VGA is an amplification element whose gain can be variated by means of a control signal. The control signal may be either an analog voltage or a digital signal. It has the function to control the output power of the transmitter. (See Figure 4.8).

Power Amplifier

This is the last stage of the transmitter, it provides the signal with the last amplification. The power amplifier or PA has the capability to drive high power demanding loads. In this case it provides the antenna with a high power signal that can be radiated to the tag. (See Figure 4.8).

Filter

After the power amplifier the bandwidth of the signal is limited in order to eliminate the inter modulation products resulting from the amplification process.

Figure 4.9 shows a picture of the transmitter PCB (Printed Circuit Board). The transmitter board can be connected directly to the Virtex™ 6 evaluation board through a high-speed digital interface.

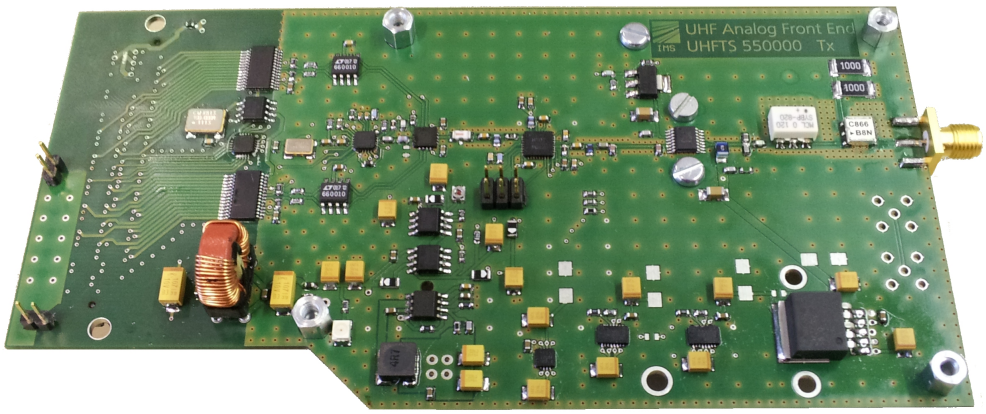

Figure 4.9: Complete Transmitter Board with FPGA Interface

4.4 Test Tag

This thesis is basically focused to the physical link of RFID systems. A test tag allows to determine when and what is received, without the interference of protocol related influences. Figure 4.10 shows the block diagram of the test tag. The test tag can be programmed to constantly send a specific frame or use an external signal for the modulation.

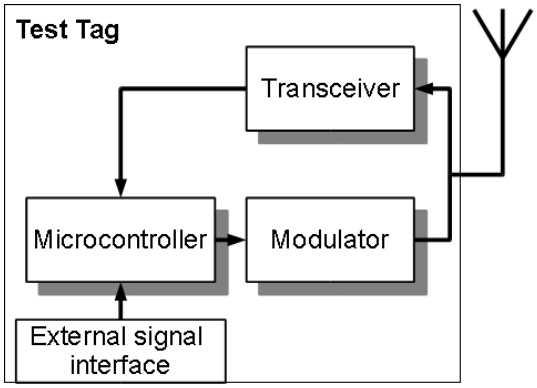

Figure 4.10: Block Diagram of the Test Transponder

4.5 PC Interface

The test platform can be configured and controlled from a PC through a USB connection. The PC has full communication with the test platform, it can request and ask information about a specific events.

4.5.1 Module Description

The signal processing modules can be described using either VHDL or Verilog. The ISE Design Suit software from Xilinx^{TM}offers a complete environment for logic description. Basically any HDL generator compatible with Xilinx^{TM}devices can be used.

4.5.2 Configuration

The FPGA configuration is made via the USB-JTAG port. This interface is also used for the ChipScope communication.

4.5.3 PC Communication

The test platform includes an USB-Serial module that allows to connect the Board to the PC through an USB port. This interface can be used to communicate with FPGA by means of a serial terminal.

Datapoints and Parameters: There is a data communication bus implemented in the system. Basically there are two memory arrays: one for control and one for status. The registers in the control arrays are input signals or parameters into the system, whereas the status array are output signals of the system. These two memory array can be used to configure a module, trigger a task of to get information out of the system.

Protocol: The PC can write data into the control array and in the same way read data out of the status array. The protocol is simple, the first byte in a message tells the data bus whether to write or read, the second byte tells how many bytes and a third byte gives the address of the memory array.

4.5.4 Visualization

ChipScope: "ChipScope tool inserts logic analyzer, system analyzer, and virtual I/O low-profile software cores directly into the design, allowing to view any internal signal or node, including embedded hard or soft processors. Signals are captured in the system at the speed of operation and brought out through the programming interface. Captured signals are then displayed and analyzed using the ChipScope Pro Analyzer tool". [4]

Test-points: The communication interface in the test board can be used to transfer data to the PC. A VHDL module allows the storage and latter transfer the data of a test point in the system. In this way test-points can be added internally in the system and visualized in the PC.

Chapter 5

New Approaches

5.1 Under-Sampling in UHF RFID

As already mention in section 2.3.1, there are other sampling schemes that allow to sample signals with frequency components higher than the double of the sample frequency. This sampling scheme is used for the digitization block of the software-based UHF RFID system presented in this work.

5.1.1 Principle

Under-sampling or bandpass-sampling is based on the condition that the signal is bandwidth limited and periodic. If the signal spectrum has no frequency components below f_{min} and over f_{max}, then after equation 2.1, the sampling frequency should be at least two times the bandwidth of the signal.

By under-sampling a signal, replicas of the complete bandwidth are created. The replica that appears bellow $\frac{f_s}{2}$ is the one that is further used.

When a signal is samplingd, this can be represented mathematically as the multiplication of the signal by a train of Dirac-pulses. Equation 5.1.

$$x'[t] = x(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - n \cdot \frac{1}{f_s}) \tag{5.1}$$

This means replicas of the signal spectrum appears every $n \cdot f_s$. Equation 5.2.

$$X'[f] = X(f) * \sum_{n=-\infty}^{\infty} \delta(f - n \cdot f_s) \tag{5.2}$$

Taking advantages of this replicas we can choose an $f_s < 2 \cdot f_{max}$ that creates a replica in a lower frequency band below $\frac{f_s}{2}$, see Figure 5.1

The theory and conditions for the under-sampling are well documented in [51] [70] [42], but they are basically given by

$$\frac{2 \cdot f_{max}}{n+1} \leqq f_s \leqq \frac{2 \cdot f_{min}}{n} \tag{5.3}$$

where

$$n \leqq \lfloor \frac{f_{min}}{f_{max} - f_{min}} \rfloor \tag{5.4}$$

"n" is the number of replicas between 0 and the central frequency of the bandpass signal.

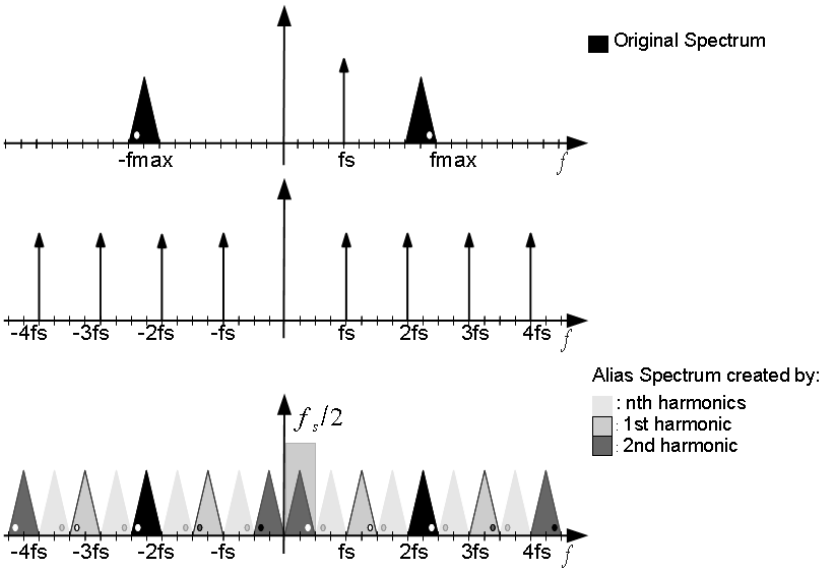

Figure 5.1: Undersampling Scheme Example [36]

Figure 5.1 shows the frequency spectrum of the bandpass signal after the under-sampling, for this case $f_{min} = 8$ and $f_{max} = 10$. After equation 5.4: $n \leqq 4$, with $n = 4$ the sampling frequency can be calculated after equation 5.3: $5 \leqq f(4) \leqq 4$, hence in Figure 5.1 $fs = 4$. The original spectrum is drawn in black and the circle in every triangle indicates the sign of the frequency spectrum (right = positive and vice versa). The alias generated by the second harmonic of f_s (dark gray) is the one that appears in the $f \leqq \frac{f_s}{2}$ zone, and the one considered as sampled signal.

Advantages of Under-sampling

The advantages and characteristics of under-sampling have been well studied and explored in [32], [51], [42], [36]. The most important characteristics is that the signal digitization and frequency conversion take place in a single process.

By using an under-sampling scheme the system could be reduced in complexity by eliminating the extra frequency conversion and filters, thus allowing to realize the signal processing in the digital domain in an earlier stage. See Figure 2.3

5.1.2 Simulation

Before this sampling approach is implemented as the digitization block, a simulation using Matlab^{TM}[2] was made in order to test its feasibility. The simulation model used in section 3.2 is further used to test the under-sampling scheme in UHF RFID signals.

The signal used is the one at the input of the demodulator, see Figure 3.7. At this point the signal has been modulated and received back by the reader. The information signal is a query command and it is FM0 coded. The data rate or BLF (Backscatter Link Frequency) is 156.25 KHz.

Choosing the Sampling Frequency

The selection of the sampling frequency is very important for a correct sampling of the signal. It does not only depend on the relation given by equation 5.3, but on the precision of the clock used to sample. The higher the bandpass signal is situated regarding the origin the smaller the limits for f_s, for a given n, are. Choosing an f_s close to the theoretical minimum will require a high precision clock, any tolerances will drive the f_s to forbidden values. Therefore an f_s greater than the theoretical minimum is recommend [70].

For the simulation the signal is passed through a bandpass filter with a bandwidth of 20 MHz centered on 860 MHz, this filter covers the frequencies allowed for Europe. The 3 dB limits of the bandpass filter were used to calculate n, using the equation 5.4.

$$n \leqq \lfloor \frac{850}{20} \rfloor = 42 \tag{5.5}$$

The bandpass filter functions not only as an anti-aliasing filter, it also creates a *guard band* between positions where the spectrum could be aliased [70]. The resulting overall 3 dB bandwidth places the signal in a so called half integer band position; the

bandpass signal is located at an integral number plus a half of the bandwidth. This allows an effective relocation of the bandpass signal.

Choosing the limits of the bandpass filter for the calculation gives a higher f_s than the theoretical minimum. This is recommended in order avoid aliasing due to clock tolerances or engineering imperfections. For a detailed description see [70]. The chosen frequency was taken out of the interval given by n=42, after equation 5.3

$$41.4286 \cdot 10^6 \leqq f_s \leqq 41.4634 \cdot 10^6 \quad Hz \tag{5.6}$$

This interval gives enough room for clock imperfections. The results of the simulation are shown and discussed in 7.2.1.

5.1.3 Implementation

Undersampling in UHF RFID Systems

The advantages of the under-sampling can be applied to the UHF RFID systems achieving the digitization and the frequency translation of the signal in a single stage, thus avoiding the need of a complex analog front-end and hardware elements. Hence the signal processing could take place in the digital domain in a earlier state of the system.

Requirements

There are certain conditions that need to be fulfilled in order to under-sample the UHF signals in RFID systems successfully:

Carrier Suppression: One of the biggest challenges in RFID Systems is the relation between the carrier and the signal being reflected by the tag. The last one containing the actual information. The level of the carrier is usually higher than the level of the reflected signal. For a full digitization, it would be necessary to have an ADC with a high bit resolution in order to keep the quantization step small enough to avoid the information signal from getting lost in the quantization process. With the existing ADC technology it is not possible to fulfill this requirement. Therefore a carrier suppression block must be placed before the digitization takes place. The isolation factor of the carrier decoupling circuit determines the sensitivity, which is directly proportional to the carrier isolation in this case. The dynamic range of the ADC determines the smallest signal that can be digitized for a given carrier level. See Figure 5.2.

The graphic is calculated for an output power of 20 dBm, the ideal dynamic range of the ADC can be calculated with equation 5.7. The Figure 5.2 shows the minimal signal power (or sensitivity) that can be achieved by a given ADC vs the carrier isolation.

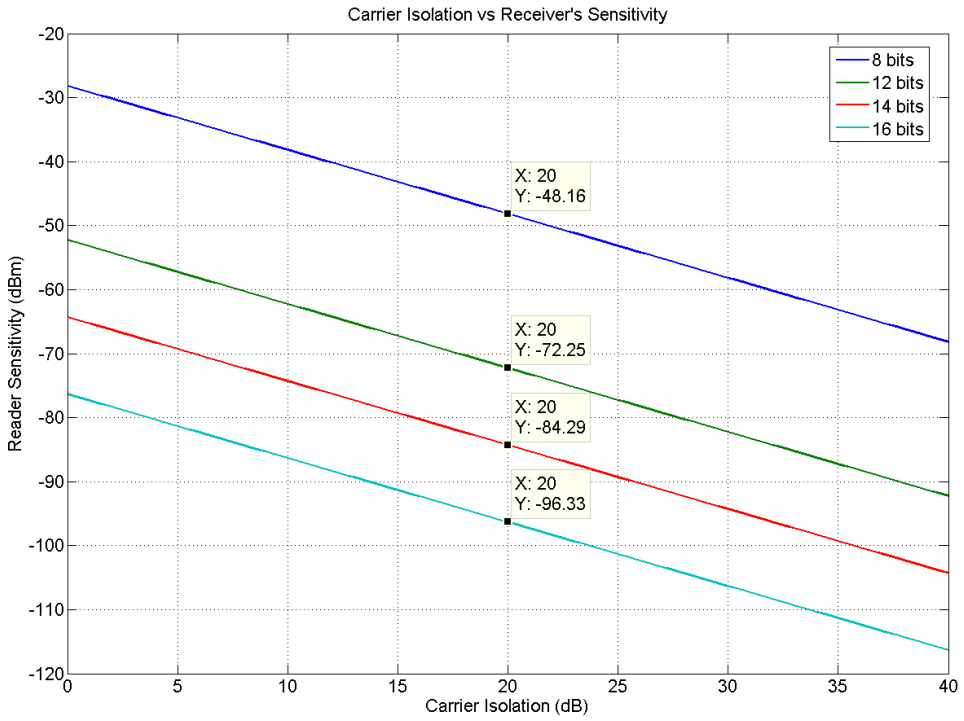

Figure 5.2: Receiver's Sensitivity vs Carrier Isolation: According to the carrier isolation, the maximum receiver sensitivity can be determined for each ADC bit resolution

$$DynamicRange = 20 \cdot log_{10}(2^n) \tag{5.7}$$

The markers in Figure 5.2 show the 0 dB line, i.e. the isolation is 20 dB which is the typical value of a single circulator. The carrier suppression circuit used for the hardware implementation is the double circulator circuit presented in section 4.2.

Bandpass Filtering: The signal needs to be bandwidth-limited in order to avoid undesired aliasing of signals outside the desired bandwidth. Therefore a bandpass filter needs to be placed before the ADC.

Amplification: In order to take advantage of the complete dynamic range and bit resolution of the ADC, the power of the received signal is increased by an amplification

step. Hence assuring a complete use of all the quantization steps and avoiding losses due to quantization errors.

Analog Bandwidth: An important characteristic the ADC should possess is a large analog bandwidth. Although the sampling frequency is quite smaller than the frequency of the signal, the ADC should be able to accept signals with frequencies up to 900 MHz with minimum distortions.

Under-sampling with Test Platform

The test platform (Chapter 4) can be configured to work with an under-sampling scheme. The two circulator decoupling board is used for the carrier suppression. The isolation is good enough to sample the RX signal with the 12-bits ADC. A bandpass filter is used to select the channel, it has a bandwidth of 20 MHz centered at 860 MHz. The 12-bit ADC module can sample signals with frequencies up to 1.2 GHz. The results of the implementation are shown in section 7.2.3.

5.2 Digital Receiver

Once having the signal in the digital domain the first task is to define an architecture for the digital receiver. Based on the under-sampling concept the signal after the ADC is a bandpass signal with a new carrier frequency, or IF (Intermediate Frequency), that can be calculated with equation 7.1. Now it is possible to test and implement different kind of receiver architectures since all processing elements are defined in software. Figure 5.3 shows the block diagram of the digital receiver.

5.2.1 Sampling Frequency

The 12-bit ADC module has a maximum sampling frequency of 550 MHz, which offers flexibility for the sampling process. Frequencies close to the theoretical limit increase the noise of the signal. Therefore it is better to calculate the sample frequency with higher n values (see equation 5.3). Frequencies around 300 MHz have proved to give good results. Figure 5.4 shows a comparison of two sampling tests; a signal sampled at two different frequencies. The bottom-left plot shows the frequency spectrum of the signal sampled at 349 MHz and the bottom-right one the frequency spectrum of the same signal sampled at 42 MHz.

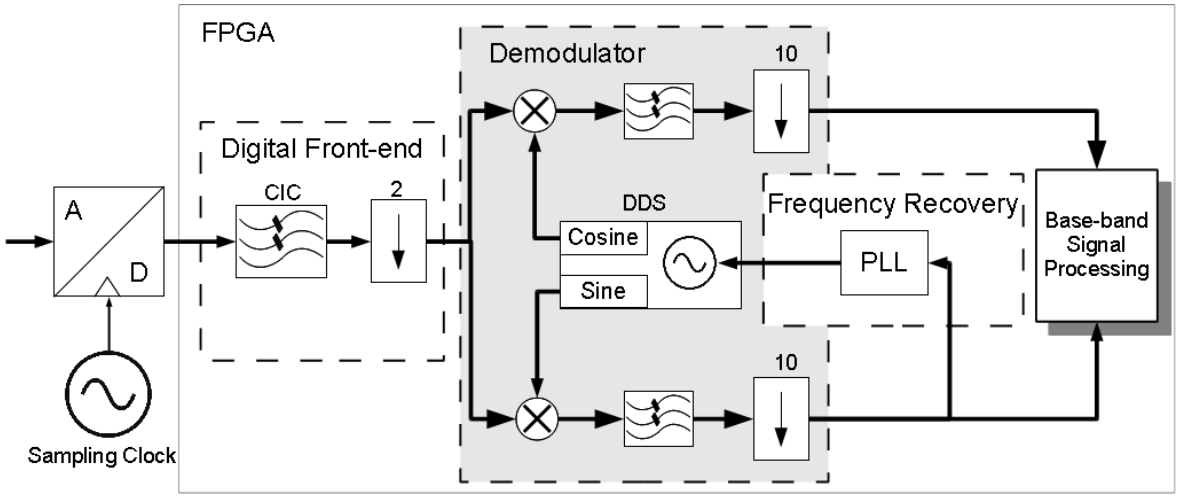

Figure 5.3: Digital Receiver Block Diagram

It can be seen from Figure 5.4 how the noise floor of the signal sampled at 42 MHz (bottom-right), is about 20 dB higher compared to the noise floor on of the signal sampled at 349 MHz (bottom-left). Equation 5.8 can be used to calculate the SNR decrease [70].

$$D_{SNR} = 10 \cdot \log(n) \tag{5.8}$$

Only a few side lobes of the baseband signal can be seen over the noise on the bottom-right plot, while on the bottom-left plot more of the baseband frequency elements can be seen. It is important to note that both of the frequency spectra show the same bandwidth and the same scaling on the y-axis.

5.2.2 Digital Front-End

There are a few processes the signal needs to go through before the demodulation. These processes form the digital front-end; in order to take advantages of the under-sampling scheme a dedicated digital front-end was developed. Figure 5.3 shows the block diagram of the digital front-end. This work was presented in [37].

Decimation

In a digital communication system the bandwidth of the received signal is typically smaller than the resulting bandwidth after the sampling process. This bandwidth is called the *Nyquist Bandwidth* and it corresponds to $\frac{f_s}{2}$. Therefore the first step on

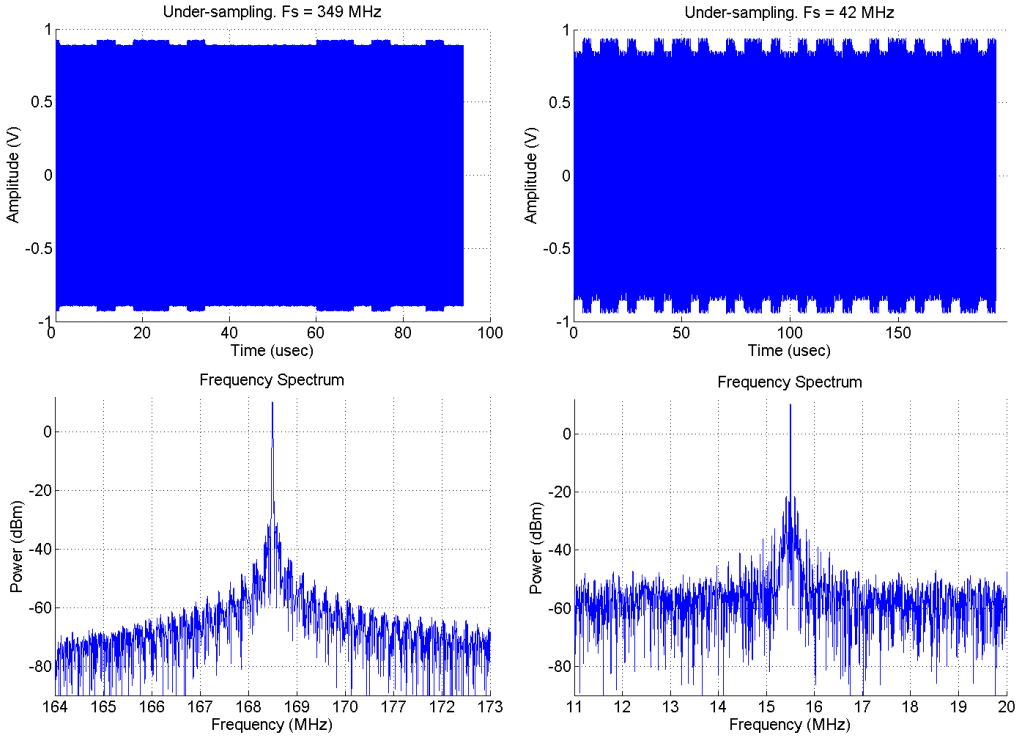

Figure 5.4: Comparison of Noise Level at 2 Different Sample Frequencies: The signal sampled at 42 MHz has a higher noise level than the one sampled at 349 MHz

a digital receiver is a decimation block, this one re-sample the received signal with a slower sample frequency. In other words it discards a certain number of samples out of the received signal. The CIC (Cascade Integrator Comb) is a digital filter structure with a lowpass filter frequency response. This filter has no need of multiplication elements, which makes it an optimal structure for decimation. The reader is directed to [51] and [39] for more information on CIC filters.

Implementation

CIC filter structures can be used directly out of the Xilinx^{TM} libraries. All parameters can be configured within a graphical environment. Nevertheless a VHDL module for CIC filters is provided, by the author of this work, that can be used with the test platform.

Demodulator

The received signal can be ASK or BPSK modulated. Therefore an In-phase/Quadrature (I-Q) demodulator is used. The I-Q demodulator provides a coherent measurement of the phase and magnitude of sinusoidal signals [51].

The basic structure of the I-Q demodulator can be seen in Figure 5.5

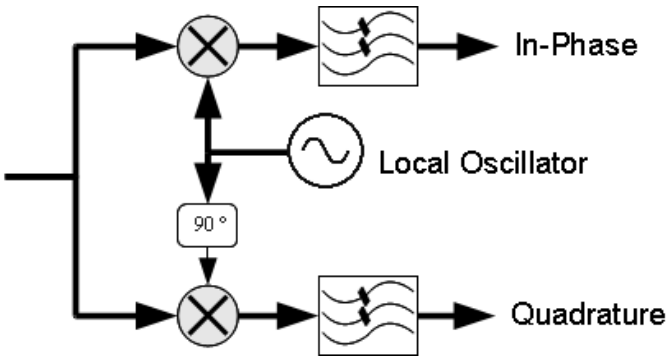

Figure 5.5: Structure of the I-Q Demodulator

Implementation: It requires two multipliers, an oscillator and phase shift element for the 90° shifted signal. The FPGA has dedicated hardware multipliers that can be used directly. For the oscillator an element called DDS (Direct Digital Synthesizer) is used. The DDS is taken from the Xilinx™ libraries, it generates sinusoid signals with a configurable frequency. The DDS provides directly a cosine and sine signals that can be used to generate the I and Q paths.

Lowpass Filter

The lowpass filter eliminates the harmonics that are generated by the multiplication of two sinusoids. It is implemented using the FIR (Finite Impulse Response) generator from the Xilinx™ libraries. The filter is also used as a decimator and for limiting the signal bandwidth after the demodulator. Hence the signal can be re-sample to a lower frequency relaxing the processing requirements of the further processing blocks.

The lowpass filter increases the SNR of the signal by liming the bandwidth of it. The noise power depends on the bandwidth of the signal, the better the lowpass filter is the less noise is let through.

Frequency Recovery

The I-Q demodulator is a coherent demodulator. Therefore it requires to know the frequency of the carrier signal in advance, the phase is irrelevant since it is contained in the I and Q paths. In a typical UHF RFID reader the carrier frequency signal is well known, since it is the same one used for the generation of the electromagnetic field that provides the tag with energy. Nevertheless after the under-sampling process the frequency of the carrier signal is changed. Even though it can be calculated, the exact value is unknown. A frequency recover element is necessary. Here a PLL (Phase Locked Loop) is used. A PLL is basically a control loop that regulates the frequency of an oscillator in order to match the frequency of a reference signal [15], in this case the carrier. Figure 5.6 shows the block diagram of the implemented PLL.

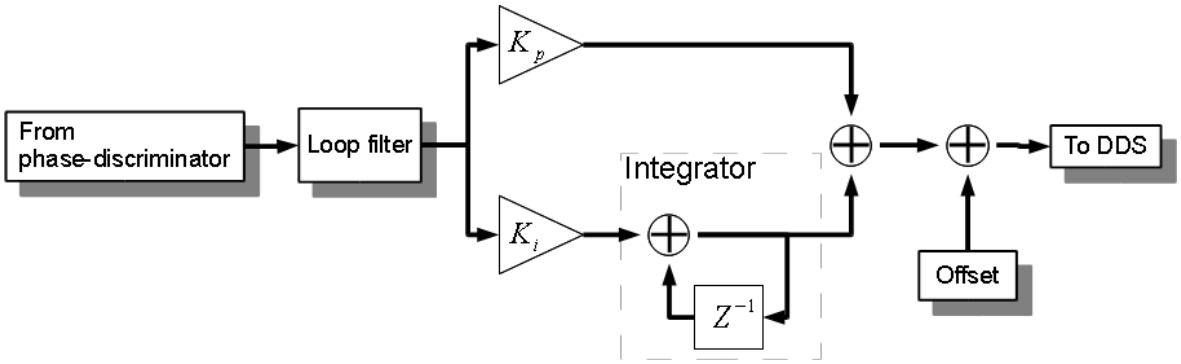

Figure 5.6: PLL Block Diagram

Implementation: The quadrature (Q) path is used as phase discriminator, the PLL regulates the DDS until the quadrature path converges to 0. In other words, when the phase of the carrier and the one from the DDS are the same, the DC offset of the quadrature signal is zero. This structure keeps the DDS at the same frequency as the incoming carrier. The PLL is programed in VHDL, the modules are configurable and can be used in different arranges. (See Figure 5.6).

5.3 Full Symbol Correlation

It was shown in section 3.3.1 how the FM0 symbols are orthogonal to each other and the Miller 2 to Miller 8 symbols are not. Due to its non-orthogonality, the cross correlation

of the Miller symbols does not result in a maximum euclidean distance. Nevertheless a correlation receiver can take advantage of the Miller symbol length in order to improve the signal-to-noise-ratio (SNR) of the signal. Different to the approaches presented in [12] and [65], this approach uses the complete symbol length for the receiver filter.

Although this may be a theoretical best-choice the implementation may require more processing resources than other correlators, specially when different data rates are supported.

5.3.1 Simulation

The full symbol correlator is first tested using the simulation model presented in section 3.2. More details are presented in section 7.3. The advantages of this receiver are clearly seen in the test that take place in section 7.5.2.

5.3.2 Implementation

By taking advantages of the new FPGA technology this approach can be implemented and optimized to consume the less resources as possible. In this work a full correlation receiver was implemented in hardware, using the test platform, the results will be presented in 7.3. Two FIR filters are used for the correlation receiver, one to search for symbols representing $0s$ and the second one to search for symbols representing $1s$. The length of the FIR depends on the sample rate of the baseband signal. The filter final length results by building the FIR coefficients for the Miller 8 symbols. In this way the filter can be used for shorter symbols (Miller 4, Miller 2 and FM0) as well. Figure 5.7 shows the resulting correlation filters for the different symbol forms.

The filter coefficients can be either +1 or -1. When the remaining coefficients are not used these are left to be 0, in this way the extra length of the filter does not influence the correlator output. The different filter coefficients for the different symbol forms are stored in memory and can be loaded in the FIR filter as required. This allows to use one single FIR filter for all symbol forms.

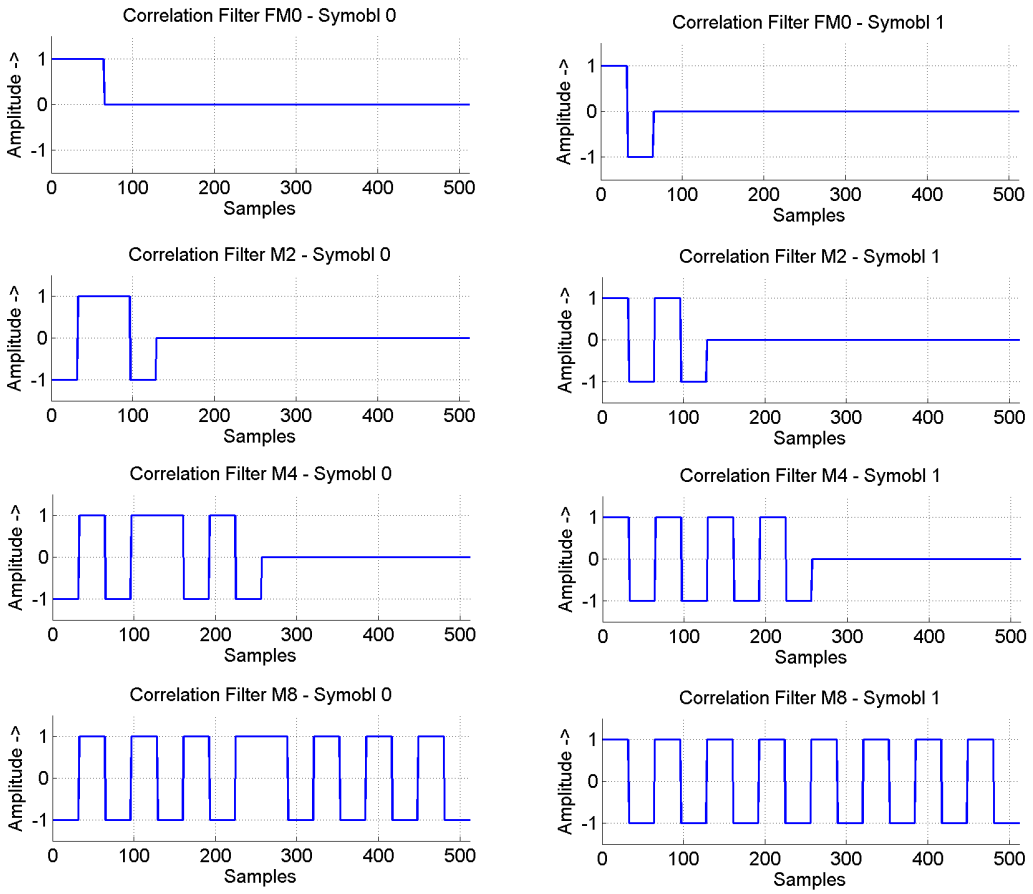

Figure 5.7: Correlation Filters

5.4 New Coding Scheme

After implementing a full miller correlation it was observed that the miller symbols present little orthogonality to each other. In other words their cross correlation is not optimal for a reliable bit recognition. Figure 3.9 shows the cross correlation of the different Miller symbols.

It can be seen that the peaks besides the center one are relative high compare to it. Another encoding scheme that presents a better cross correlation and hence a higher correlation gain could be used. A potential improvement of the system is recognized.

5.4.1 Pseudorandom Noise Based Coding Scheme

A pseudorandom noise (PN) sequence is a signal with similar characteristics to noise, it satisfies one or more of the noise statistical randomness. PN coding is used in spread

spectrum systems where the receiver correlates a locally generated signal with the received one. At the receiver side the local sequence has a very low correlation with [35]:

- any other sequence in the set
- the same sequence at a significantly different time offset
- a narrow band interference
- thermal noise

It was decided to use gold sequences for test and implementation purposes. Gold sequences are binary sequences of length $2^n - 1$ with a small cross correlation between sequences. This makes them convenient for digital signal transmissions. But other PN sequences can be used as well. The length is measured in number of chips, each binary element in the sequence is a chip. This approach was presented in [35].

Sequences of different lengths were tested and compared against the UHF RFID standard coding scheme, the results would be shown in section 7.3.

Simulation

In order to analyze the characteristics of the coding schemes, a simulation of the entire system was done using Matlab™ [2]. The simulation model presented in section 3.2 is changed to encode the tag signal with different gold sequences of different lengths. The simulation model was extended and a Maximum-Likelihood decision maker was implemented. It is basically a matched-filter receiver that correlates the incoming signal with the possible symbols forms, the correlator outputs are sampled at the symbol rate and compared to each other. The simulation is used to compare the EPCglobal Gen2 coding scheme against the presented PN codes.

Bit-Error-Rate Test: The comparison was made by obtaining the BER at different SNR values and for different codes. The length of the used Gold sequences were chosen as follow:

- gold sequence length 3 as a substitute for Miller 2
- gold sequence length 7 as a substitute for Miller 4

- gold sequence length 15 as a substitute for Miller 8

In this way the symbol lengths of the Gold sequences are comparable to the Miller symbols; considering the half of an FM0 code as a chip. Two Gold sequences for each substitute are used, one to represent a "1" and the other a "0". To measure the BER, 100 000 random bits were sent for each encoding scheme and at different SNR values. The SNR is set by simply increasing the added noise. The results of the simulation are presented and analyzed in section 7.3.

Hardware Implementation

In order to confirm the results, as well as to prove the feasibility of PN codes in UHF RFID, a test system was implemented in the hardware platform and the test transponder presented in chapter 4.

Bit-Error-Rate Test: The bit-error-rate test was repeated under the same conditions as for the simulation. 8 random bits are generated in Matlab^{TM}, these ones are transferred to the FPGA where they are encoded. The encoded signal is used by a test tag to switch the matching circuit of the antenna. This creates a backscatter signal that is received by the hardware platform. See Figure 5.8.

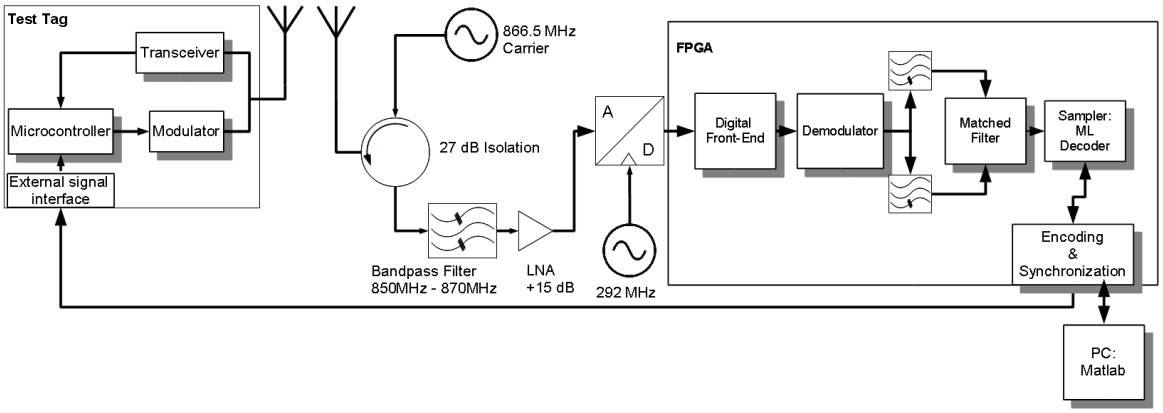

Figure 5.8: BER Test Block Diagram

In order to decode and recognize the symbols sent by the tag, the baseband signal is correlated with the possible symbol forms. Thereafter the signal is sampled at the symbol rate. The correlation that provides the maximum output value determines which symbol was sent. The received binary data is transferred back to Matlab^{TM} where

it is compared with the sent data in order to find possible errors in the transmission. This procedure is repeated 12500 times for each of the gold codes and miller symbols at different SNR values. The SNR setting was done by changing the power of the CW. The results of the measurement are presented and analyzed in section 7.3.

5.4.2 Orthogonality Test

The orthogonality of the gold sequences increases with the rising length. There are $2^n - 1$ possible orthogonal sequences in a set, each one consisting of $2^n - 1$ chips. Short lengths present little or none orthogonality, therefore in order to demonstrate its feasibility for RFID systems, a set of sequences of length 31 was used; this is a good code length since all the sequences in the set are orthogonal enough, and the length is not too long to use it for RFID. For a digital representation the next possible power of 2, that is smaller than 31, is 16. Using 16 different sequences 4 information bits can be transmitted by one single symbol.

The same hardware platform is used to test the advantages of orthogonality. A random binary message was separated in packages of 4 bits, each package represents one symbol. There are 16 possible symbol forms, each symbol form is encoded with a gold sequence. The reader needs to correlate the received signal with all possible symbol forms. In other words there are 16 correlation filters at the receiver each one loaded with one of the 16 symbol forms. The 16 outputs are sampled at the symbol rate and the values compared to each other in order to decide which symbol was sent. To test the coding scheme a message of 64 bits was sent, i.e. 16 symbols.

Figure 5.9 shows the output of the 16 correlation filters each one plotted in a different color to facilitate the recognition of each symbol. Each peak represents the detection of a respective symbol. Only one peak is seen at the sample time.

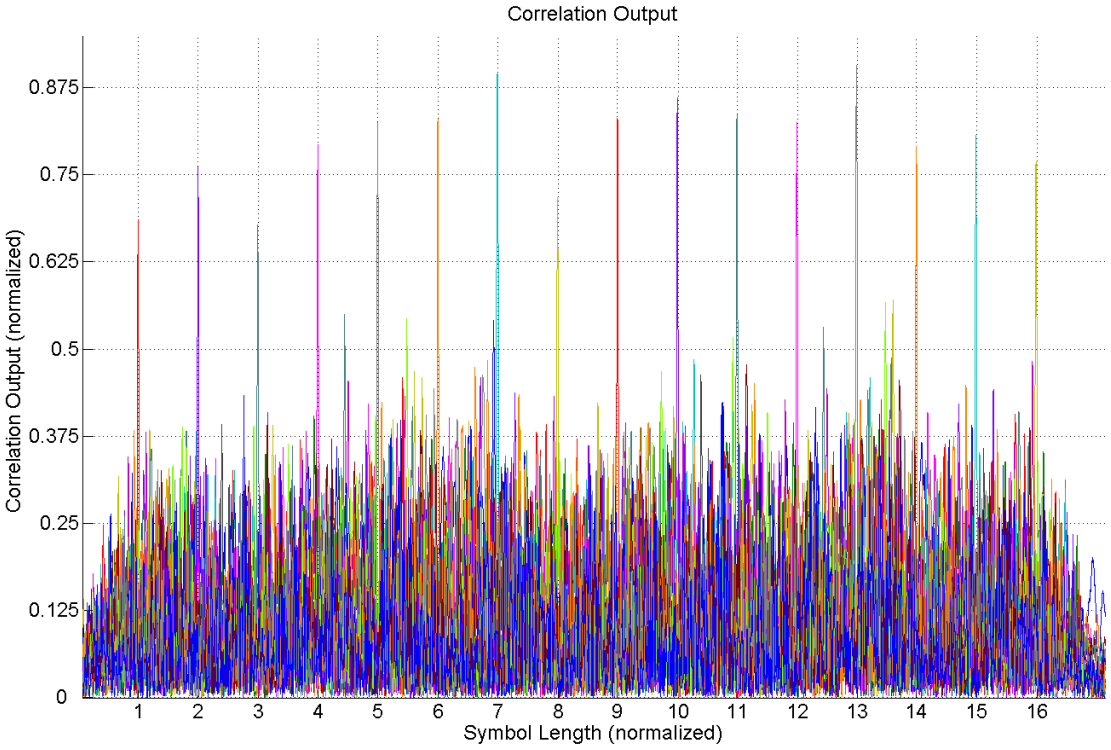

Figure 5.9: Correlation Bank Output

Chapter 6

Digital-Controlled High Isolated Carrier Suppressing System

A critical point in UHF RFID systems is the carrier decoupling or suppression. As already mentioned the carrier signal is used by the tag as power supply and to backscatter information to the reader. This signal is required during the complete communication process, hence some of the carrier signal couples into the receiver path, specially on monostatic configurations; the isolation in bistatic configurations is approx. 35 dB. The power of the carrier signal is quite higher than the backscatter signal coming from transponder, which makes the signal recovery a complex process.

The amount of carrier signal that couples depends on the type of decoupling circuit in use, and on the signal reflexions in the environment which can variate. The goal is to have a system that keeps the carrier isolation at maximum under all conditions, i.e. the required controller should be stable and fast enough to compensate for typical environment changes. In this section a novel active carrier suppressing system is presented. The research and development was made in collaboration with some colleges and students specialized in high frequency circuits [62], [61], [16].

6.1 Principle

The basic principle of the suppression systems is to take a part of the generated carrier's signal, and use it to eliminate the part of the same carrier that couples into the receiver path. Figure 6.1 shows the simplified block diagram of the suppressing system.

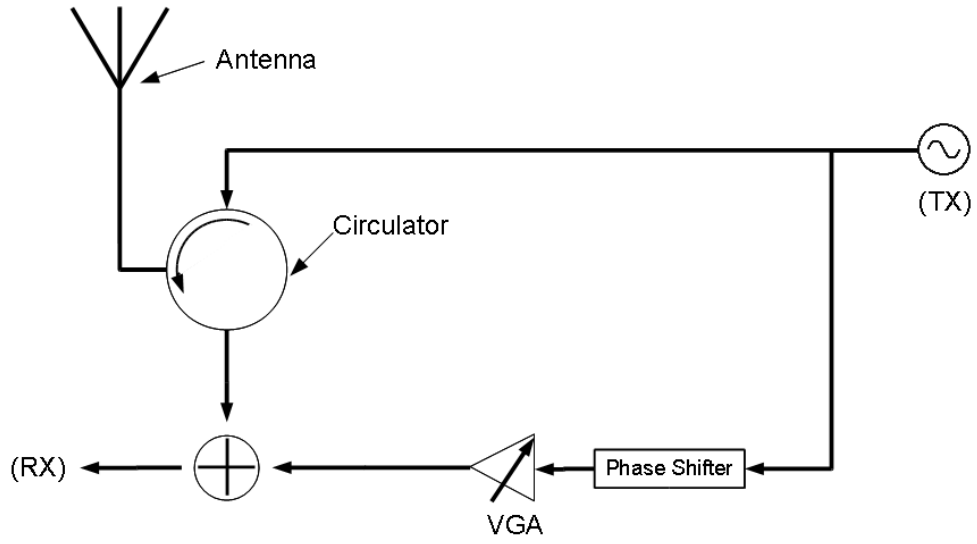

Figure 6.1: Simplified Block Diagram of the Carrier Suppressing System

This signal used to compensate the carrier at the receiver, has the same frequency but different phase and amplitude, therefore these two last parameters have to be adjusted in order to match the amplitude of the carrier and keep a phase difference of 180°.

6.2 Hardware

After research and tests an integrated hardware was developed. This circuit board integrates various elements required for the implementation and test of the proposed suppression system. The main elements of the circuit board are explained in this section. Figure 6.2 shows a detailed block diagram of the system. The following subsections explain the control and hardware elements in Figure 6.2. Nevertheless description of the hardware elements is only a basic overview, a more detailed explanation can be found in [62].

6.2.1 Routing Components

These are the elements that guide the high frequency waves through the system.

- First a small part of the original TX signal is split to be used for compensation. Figure 6.2 marker “A ”. The amplitude and phase of the split signal are regulated and then added with the RX signal. Figure 6.2 marker “B ”.

- The rest of the TX signal is passed through a circulator, here the RX is separated from the TX path. Most of the signal power is fed to the antenna, nevertheless a part is still coupled into the receiver. Reflection coming from the environment can couple into the receiver as well. The typical isolation of a circulator is 20 dB. Figure 6.2 marker "C ".

- The output of the circulator is used as reference for the compensation part. The phase and amplitude of this signal are measured and used as set point by the compensation algorithm. Figure 6.2 marker "D ".

- Finally the output of the circulator is added with the compensation signal. Figure 6.2 marker "E ".

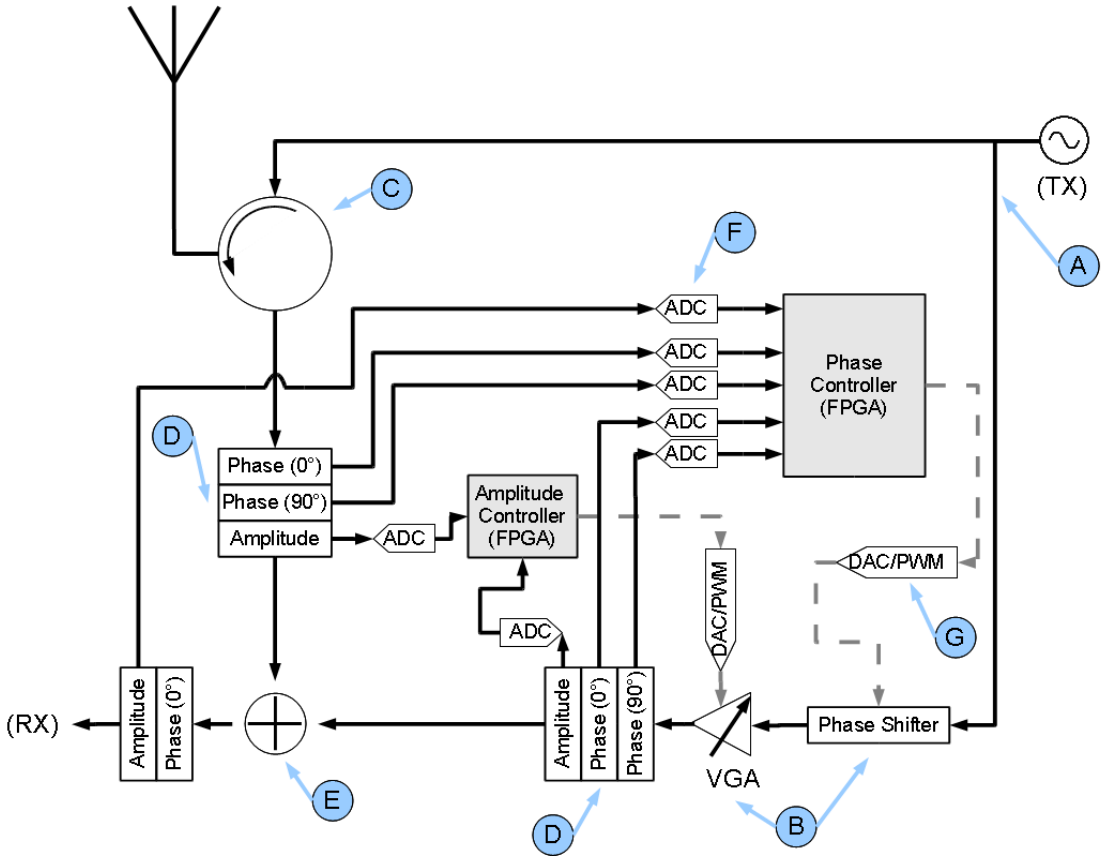

Figure 6.2: Detailed Block Diagram of the Carrier Suppressing System

6.2.2 Setting Components

These are the elements that allow the compensation system to change the phase and amplitude of the compensation signal, Marker “B ”.

- *Phase Shifter*: It is a high frequency element that can of modify the phase of a sinusoidal signals from 0°to 180°. Two of these elements are used in order to be able to shift the phase from 0°to 360°.
- *Variable Gain Amplifier*: It is a high frequency element used to increase or decrease the amplitude of a given signal. The amplification gain can be set as required.

6.2.3 Sensing Components

In order to control the system, it is necessary to have information about the phase and amplitude of all signals in it. This is done by a specialized IC (Integrated Circuit) that can measure the phase and amplitude of high frequency signals in relation to a reference signal. Figure 6.2 marker “D ”.

6.2.4 Interface to FPGA

The phase and amplitude information are delivered in form of analog voltage levels. These voltages are converted to digital by ADCs, the FPGA receives the digitized values from the ADC through an SPI interface. Figure 6.2 marker “F ”. The ADCs have a 16 bit resolution.

The setting components are both voltage controlled, the FPGA can control them by either a PWM (Phase Wave Modulation) signal or a DAC. Figure 6.2 marker “G ”.

6.3 Analysis

Once the system was completed, it was necessary to perform a system analysis. First the influence of a moving reflective object in the environment is considered. Thereafter information of the system response is necessary in order to develop an effective and feasible control algorithm. There are two control system to be considered: the phase and amplitude of the compensation signal. This section presents a summary of the system analysis, for a deeper description refer to [16].

6.3.1 Influence of a Moving Reflective Object

This analysis helps to determine how fast the controller should react to a change in the environment. For this analysis a specific environment and conditions are considered:

- The TX and RX path are decoupled by a single circulator with a fixed isolation from 20 dB. The power of the transmitter is 1 Watt or 30 dBm.
- The transmitter antenna is fixed and the gain is 0 dB for simplicity.
- The moving object is considered to be a total reflector, i.e. no absorption and it shifts the phase of the signal by 180°.
- The object moves only in one direction; away form the antenna (see Figure 6.3).
- No antenna detuning is considered for simplicity.
- The moving object start point is at distance of 1 wavelength (ca. 34.6 cm), and it finish at 2 wavelengths (ca. 69.2 cm). See Figure 6.3.

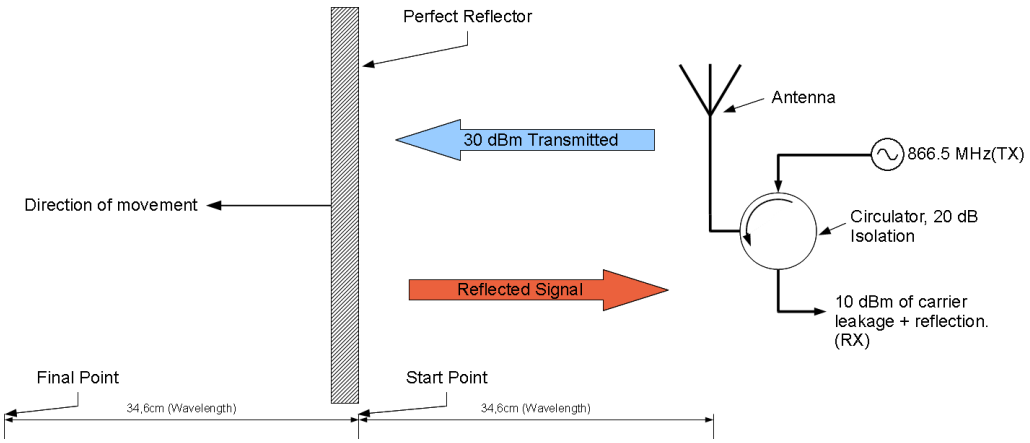

Figure 6.3: Diagram of the Environment

The power of the reflected signal can be calculated with the path loss formula 6.1, even though this formula applies only for far-field, it is used in this case for means of simplicity.

$$P_{ref} = 20log \cdot (\frac{\lambda}{4\pi \cdot d}) \tag{6.1}$$

Where λ is the wavelength and d the distance traveled by the wave. The phase of the reflected signal can be calculated with:

$$\varphi_{ref} = \frac{\frac{d}{c}}{t_c} \cdot 2\pi \tag{6.2}$$

where c is the wave propagation speed and t_c is the period of the carrier signal. Figure 6.4 shows the power of the carrier signal at the receiver against the distance the object moves from the start position away from the antenna.

In order to determine the required speed of the controller it is necessary to determine the speed of the phase and carrier amplitude change. In order do to this, a worst-case-scenario is taken: The reflector moves from 0 to $\frac{\lambda}{4} = 8.66cm$, the power of the carrier changes approx. 6.5 dB, this corresponds to a 180°phase jump (see Figure 6.4).

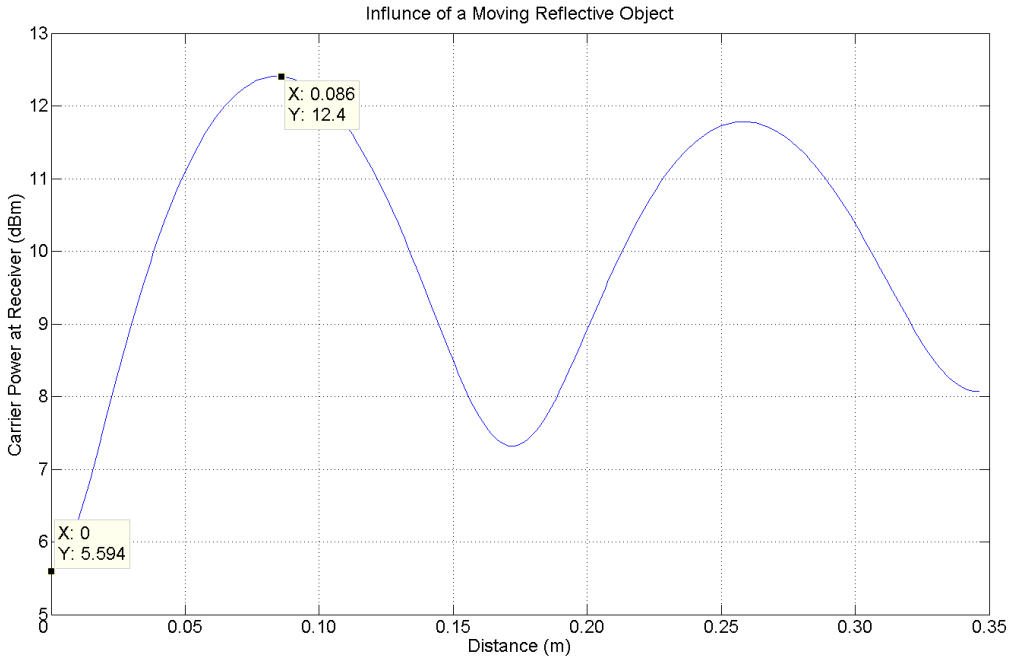

Figure 6.4: Carrier Amplitude vs Reflector Distance (referenced to the start point)

The object moves with a speed of 8 km/h or 222.22 cm/sec (typical maximum speed of a forklift), the object will cover the 8.66 cm distance in approx. 39 $msec$. The speed of the phase-change can be calculated with

$$\frac{d\varphi}{dt} = \frac{\Delta\varphi}{V_{reflector}} \tag{6.3}$$

in this case is 4.62 degrees/msec, and the speed carrier amplitude-change can be calculated with equation 6.4, in this case is 0.167 dB/msec.

$$\frac{dA}{dt} = \frac{\Delta A}{V_{reflector}} \tag{6.4}$$

6.3.2 Step Response

First the step response of the two control systems was measured. Figure 6.5 (top plot) shows the step response of the phase system. Figure 6.5 (bottom plot) shows the step response of the amplitude system.

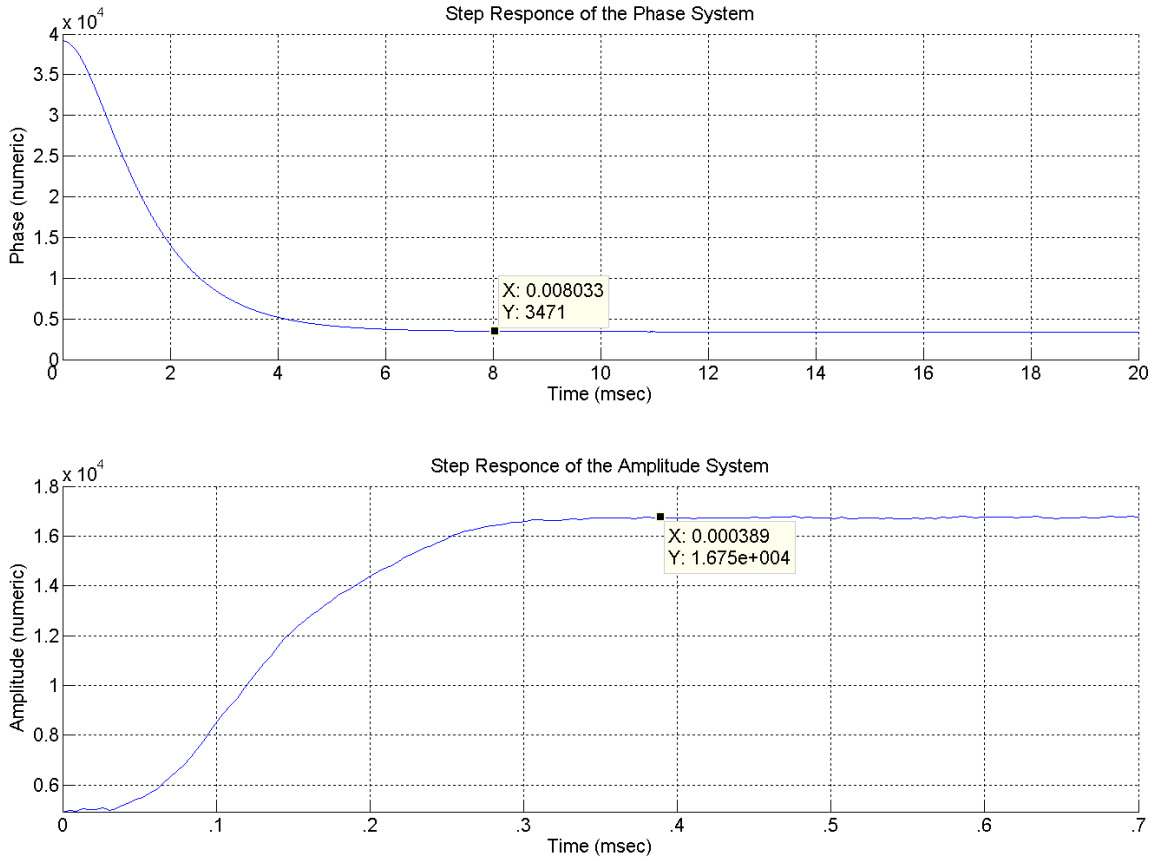

Figure 6.5: Step Responses of the Control Systems

The phase set is reached in approx. 8 *msec* while the amplitude set is reached in in approx. 400 μsec. The phase set is the slowest signal in the system, nevertheless fast enough to respond to the expected changes in the environment. According to section 6.3.1 the phase change in 8 *msec* is 36.96 degrees and the amplitude change 1.336 dB,

which is acceptable. It can be seen that both step responses present a first-order delay behavior, hence both control systems are intrinsically stable and can be regulated by a basic PI (Proportional Integrator) regulator.

6.3.3 Mutual Dependency

The dependency from one control system from the other was analyzed by measuring the response of one system when a sweep signal is applied to the other one. Figure 6.6 shows the response of the phase system at an amplitude sweep, the x-axis is given in duty cycle of the PWM signal coming from the FPGA.

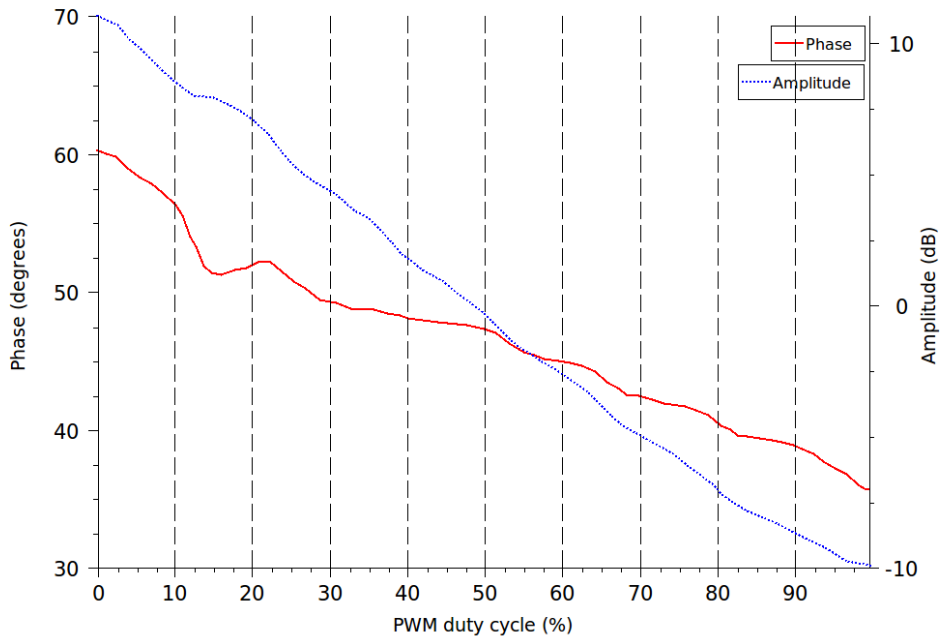

Figure 6.6: Measurement Dependency of a Signal with a Fixed Phase at an Amplitude Sweep [16]

The phase setup is fixed, the amplitude sweep is represented by the blue line, the red line is the change in the phase at given amplitude. It can be seen how the measured phase of the signal clearly changes at different amplitudes, i.e. by changing the amplitude of the signal the measured phase is also changed, this needs to be considered in the development of the control algorithm.

Figure 6.7 shows a plot with 3 phase sweeps, each one done with different signal amplitude, this figure shows clearly how the measured phase of the signal depends directly on its amplitude. The x-axis in Figure 6.7 is the setting voltage applied directly to the phase shifter.

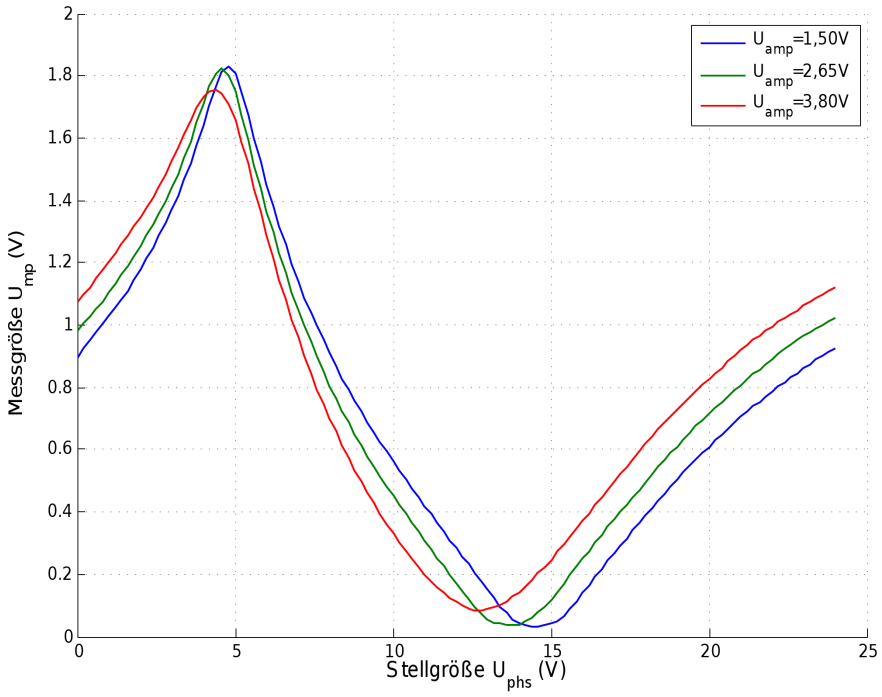

Figure 6.7: Phase sweep at Different Signal Amplitudes [62]

Figure 6.8 shows the response of the amplitude system by a phase sweep, the x-axis is given in duty cycle of the PWM signal coming from the FPGA. The amplitude setup is fixed, the phase sweep is represented by the red line, the blue line is the change of the amplitude at a given phase. It can be seen how the amplitude measurement of the signal has little dependency on the signal's phase.

Figure 6.9 shows a plot with 5 amplitude sweeps, each one with a different signal phase, it can be seen how the phase of the signal has little influence on the amplitude measurement.

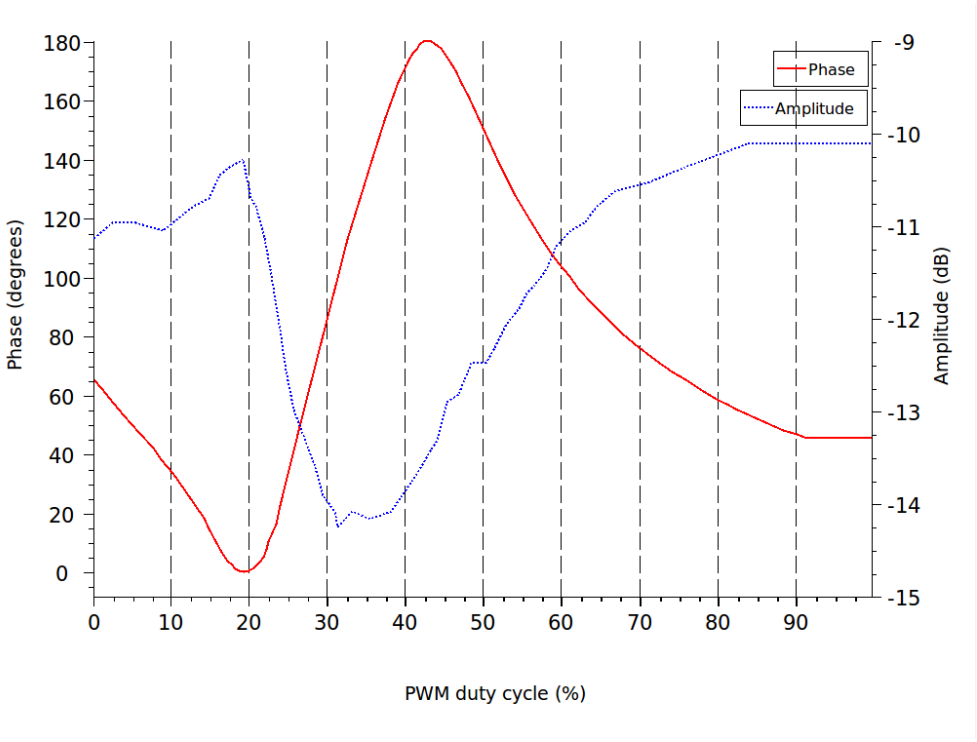

Figure 6.8: Measurement Dependency of a Signal with a Fixed Amplitude at a Phase Sweep [16]

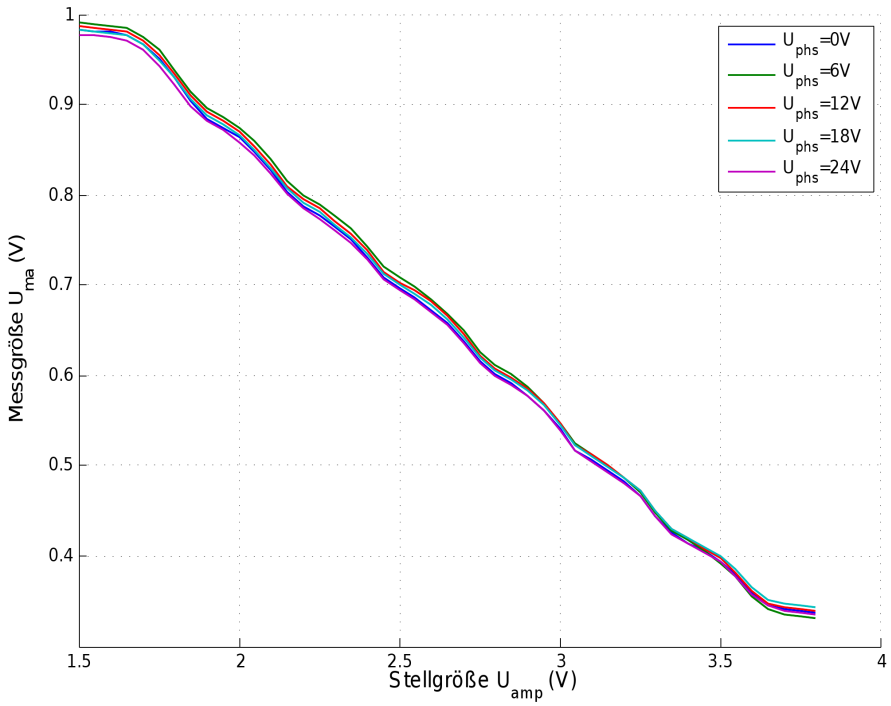

Figure 6.9: Amplitude sweep at Different Signal Phases [62]

6.4 Phase Elements

The phase control system is the most complex element, there are some special characteristics that need to be considered for the control algorithms presented in next section. This section presents the phase shifting and phase detector elements.

6.4.1 Phase Detector

The phase and amplitude measurements are made by the same IC (AD8302 from Analog Devices™). This IC is an RF/IF gain and phase detector that measures the phase and amplitude of high frequency signals compared to a reference signal. It gives the measured values as voltage levels between 0.2V and 1.8V. Figure 6.10 shows the output signal of the AD8302 gain measurement at different signal frequencies.

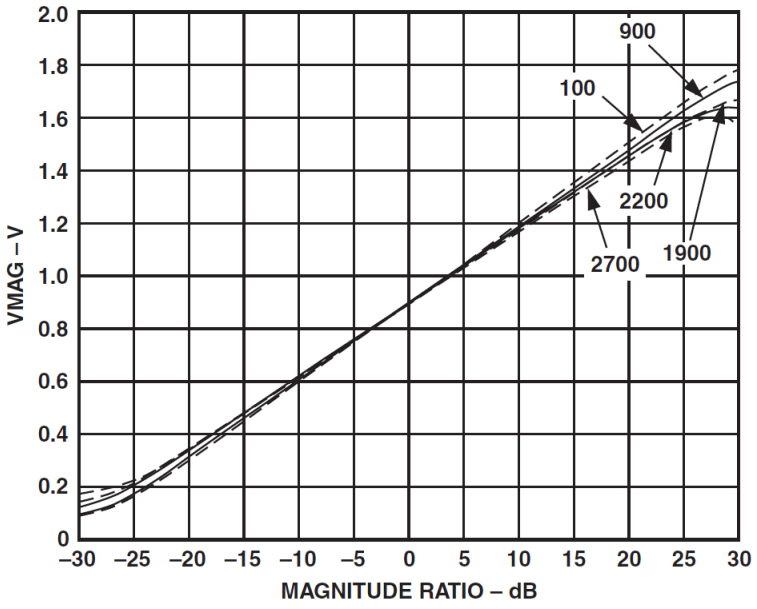

Figure 6.10: Amplitude Measuring Characteristic [23]

The response of the amplitude measurement is relative linear and does not present any problems for the control system. Figure 6.11 shows the output signal of the AD8302 phase measurement at different signal frequencies.

The AD8302 gives the same output voltage level for positive and negative phase differences. Therefore it is not possible to know the direction of a given phase shift. In order to overcome this problem the phase is measured two times, against the reference signal with a 0°shift and against the same reference signal but with a 90°shift. In this

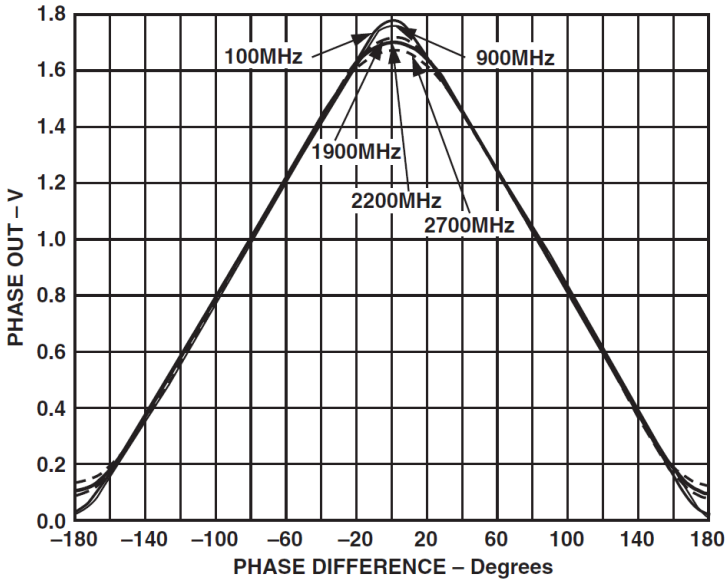

Figure 6.11: Symetric Phase Difference Measuring Characteristic [23]

way it is possible to know the actual phase of the signal. This shift on the reference signal is represented in Figure 6.2 Marker "B "as (0°) and (90°) respectively.

6.4.2 Phase Shifter

The phase of the compensation signal can be setup by a phase shift element. The degree of the phase shift can be set by a voltage level which is generated by the FPGA by means of a PWM signal. Figure 6.12 shows the phase measurement of the signal in response of a full sweep of the phase shifter.

Figure 6.12 shows the phase measurement of the signal with a 0° shifted signal as reference (blue plot) and the phase of the same signal with a 90° shifted signal as reference. From the measurement it can be recognized how the phase of the compensation signal can be changed from 0° to 360°. There are other two characteristic that can be obtained out of Figure 6.12:

- The symmetric phase-difference characteristic of the phase detector. See Figure 6.11.
- The nonlinear response of the phase shifter (this characteristic is not a measurement mistake). The phase shift does not increase linearly with the input voltage (pulse length).

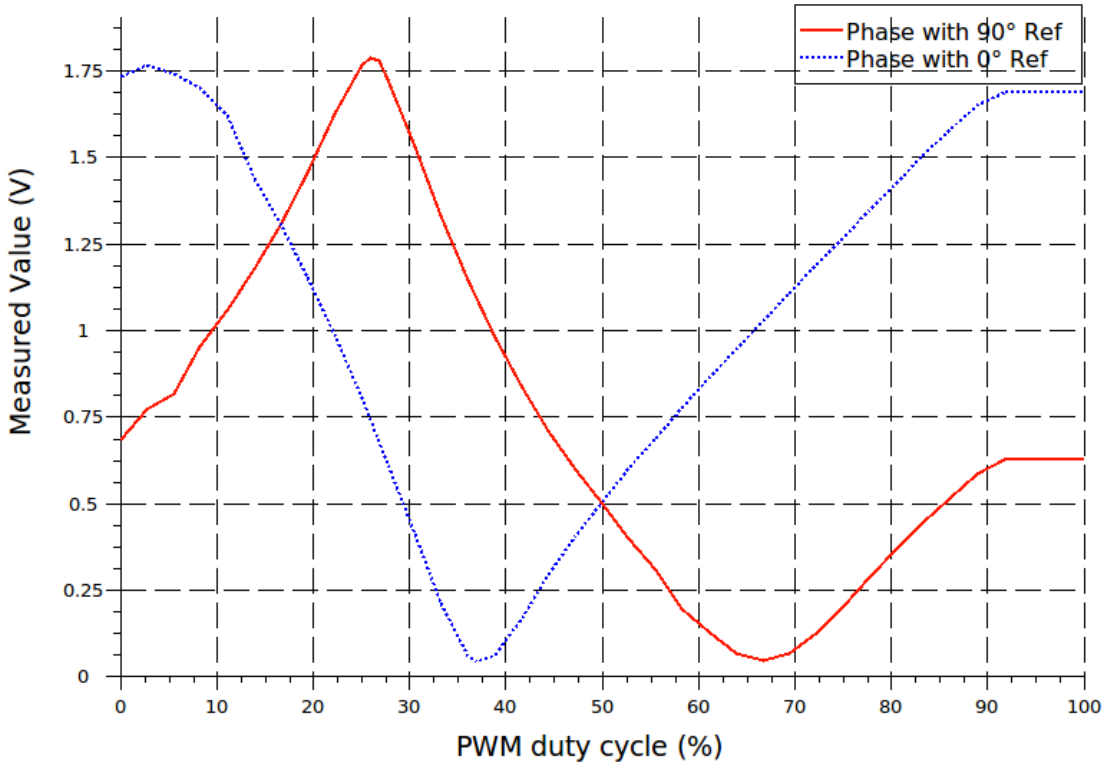

Figure 6.12: Phase sweep Response

6.4.3 Practical Minimum

The goal of the carrier suppression system is to minimize the carrier level at the receiver. A minimum leakage level can be achieved by changing the magnitude and phase of the compensation signal. Figure 6.13 shows the isolation from the carrier, in relation to the phase and amplitude of the compensation signal.

The z axis is the carrier isolation in dB in relation to the amplitude (x axis) and the phase (y axis). The carrier isolation without the carrier suppression circuit is equal to the 20 dB of the single circulator (blue line). It can be seen that there is a combination of phase and amplitude that results in a maximum isolation (minimum carrier leakage). This point is not fixed, it depends on many factors: phase of the carrier, reflexions in the environment among others. This graphic was made by making a two dimensional sweep of both phase and amplitude.

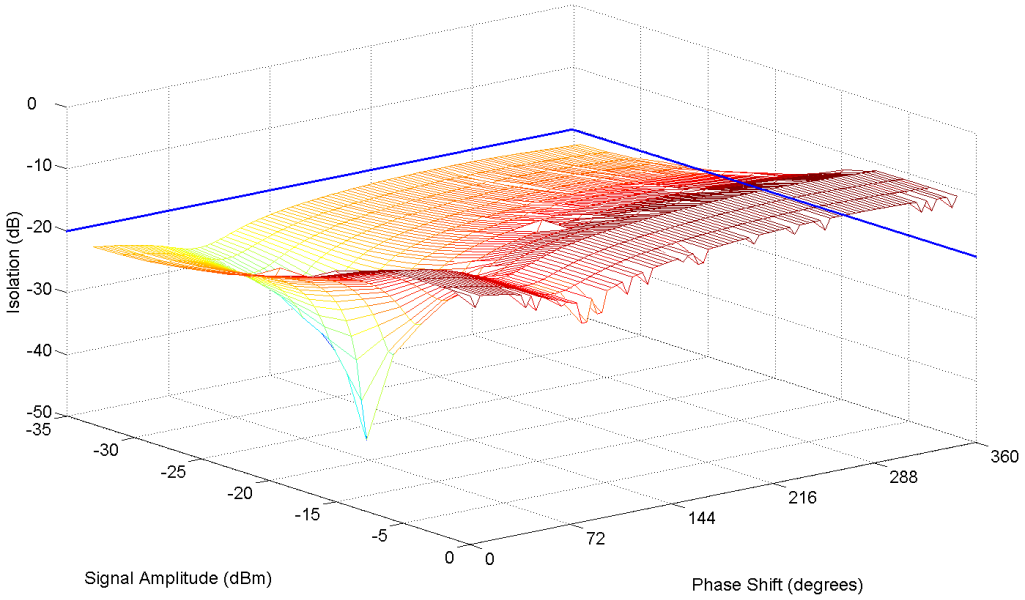

Figure 6.13: Carrier Isolation in Relation to Phase and Amplitude of the Compensation Signal [62], (tolerance $\pm 1\ dBm$)

6.5 Simulation Model

In order to understand the system and to aid the algorithm development, a simulation model was constructed by using Matlab's Simulink^{TM} [2]. The model emulates the most important elements of the system and their behavior. The simulation model is of great help to test the control algorithms before they are implemented.

6.6 Automatic Control

An automatic control is necessary since many of the parameters that influence the system are space and time variant. The system needs to be constantly adapted to the environment in order to keep the isolation to the maximum. The FPGA interface contains the control inputs and outputs, in this way different control algorithms can be implement and tested digitally. Even though the phase control system depends on the amplitude of the signal the final control algorithm can be seen as a two separated control systems. This section describes the different control modules of the carrier suppression system.

6.6.1 Amplitude Controller

The control of the amplitude is a straightforward PI regulator. Figure 6.14 shows the block diagram of the system. This block diagram is represented in Figure 6.2 as a gray box with the name *Amplitude Controller*.

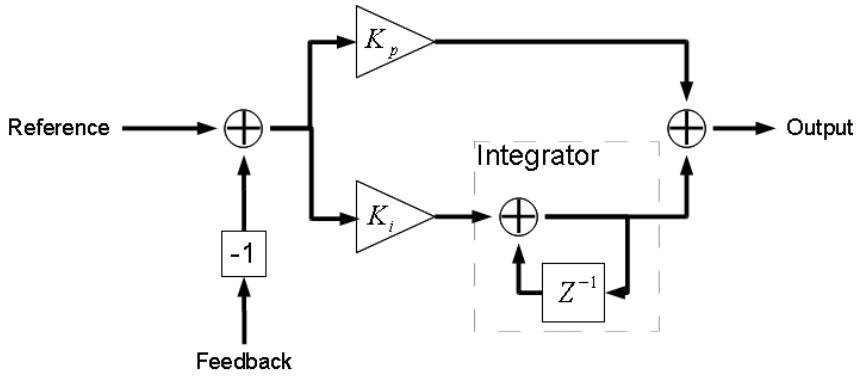

Figure 6.14: Amplitude PI-Controller Block Diagram

First the amplitude of the carrier at the receiver path is measured. This value is used as the reference value for the controller loop, in the same way the measured amplitude of the compensation signal is used as feedback for the control loop. The PI controller assures the difference of both signals is zero, in this way the amplitude of the compensation signal is coupled to the amplitude of the carrier in the receiver path. The PWM block in Figure 6.2 represents the transformation of the signal level to a pulse width.

6.6.2 Phase Controller

The phase control of the compensation signal presents a greater challenge, since it needs to be well determined in order to keep the isolation at maximum, or in other words, to keep the carrier level at minimum. The control system is explained in this section.

Challenges

- The amplitude behavior of the carrier after the addition point is periodical with the signal's phase, i.e. if a minimum is found a phase change in any direction would increase the carrier level. The controller can not know in which direction the phase has changed. This characteristic has a direct influence on the PI

controller, since the controller expects the loop error to able to take both positive and negative values. The negative values change the direction of the integrator which leads the controller to converge. A normal PI controller does not converge in this case creating an oscillating controller. See [16] for more information.

- As it was presented in section 6.4 the phase detector gives only the absolute value of the phase. In the same way the behavior of the IC is not linear, i.e. the relationship between the phase difference and the analog voltage level given by the AD8302 can not be well determined.

- The phase shift of the signal can not be set with precision. The phase shifter has a nonlinear characteristic and the phase detector depends from the signal amplitude as well. It is not possible to create a general phase-to-control-output relationship.

Figure 6.15 shows the block diagram of the phase controller. This block diagram is represented in Figure 6.2 as a gray box with the name *Phase Controller*. The elements in are described in the following sections.

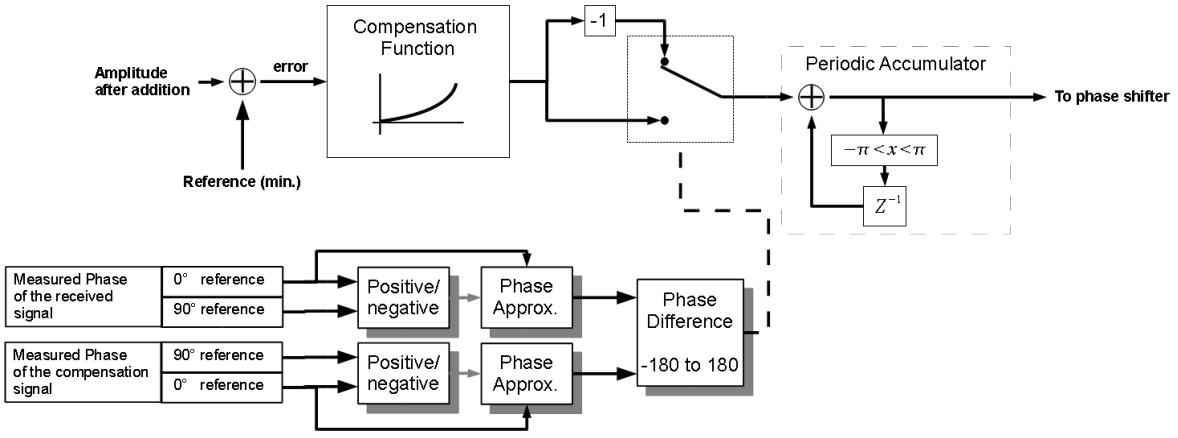

Figure 6.15: Phase Controller Block Diagram

Controller Reference: The reference value for the control loop is the minimum carrier level after the addition output, and is obtained by sweeping the phase of the compensation signal from 0° to 360°. The control converges when the difference between the reference level and the actual carrier level after the addition point are the same.

Phase Difference: The determination of the signal's phase is a complex procedure:

1: The relationship between ADC values and the phase is approximated by the relationship established out of the rising and falling curves of the phase sweep response graphic (see Figure 6.12). It is important to remark that the phase detector has a quadratic real response and not linear as shown in Figure 6.11, the behavior can be approximated with a polonium of second order.

2: Both the negative and positive phases are calculated for a measured ADC value. This is done for the 0° and 90° shifted referenced signals.

3: The phase sign is determined by comparing the calculated phase values with a phase reference. This reference, from now on called threshold, is obtained out of the graphic in Figure 6.12. The thresholds are taken out of the corresponding +90° and -90° values of both signals (0° and 90° referenced) in Figure 6.12. Figure 6.16 shows the threshold levels out of the signal curves.

The conditions are as follows: the phase is positive when

$$(\varphi_0 > TH_{0+} \cup \varphi_9 0 \geq TH_{90+}) \cap (\varphi_0 < TH_{0+} \cup \varphi_9 0 \geq TH_{90-}) \tag{6.5}$$

positive when

$$(\varphi_0 > TH_{0-} \cup \varphi_9 0 \leq TH_{90+}) \cap (\varphi_0 < TH_{0-} \cup \varphi_9 0 \leq TH_{90-}) \tag{6.6}$$

Where φ_0 and φ_{90} represent the calculated phases with reference to 0° and 90° respectively. TH stands for threshold, the 0 and 90 for either the curves with reference 0° and 90° respectively. The negative and positive sign indicates the side of the curve from which the value is taken from. Figure 6.16 shows where the thresholds are taken from.

Once the signal phases are approximated their difference is calculated. The phase difference determines the direction the phase should be compensated. The controller converges when the phase difference is kept at -180° or +180°. The phase difference works in some way as a fuzzy variable since the phase difference is only an approximation, important is whether the phase difference is negative or positive.

Gradient Descent Method: In order to add speed and accuracy to the controller the input of the periodic accumulator is calculated by a compensation function. This function gives a high compensation values for big error differences and vice versa. This creates an iteration process similar to the gradient descent method. Equation 6.7 is is

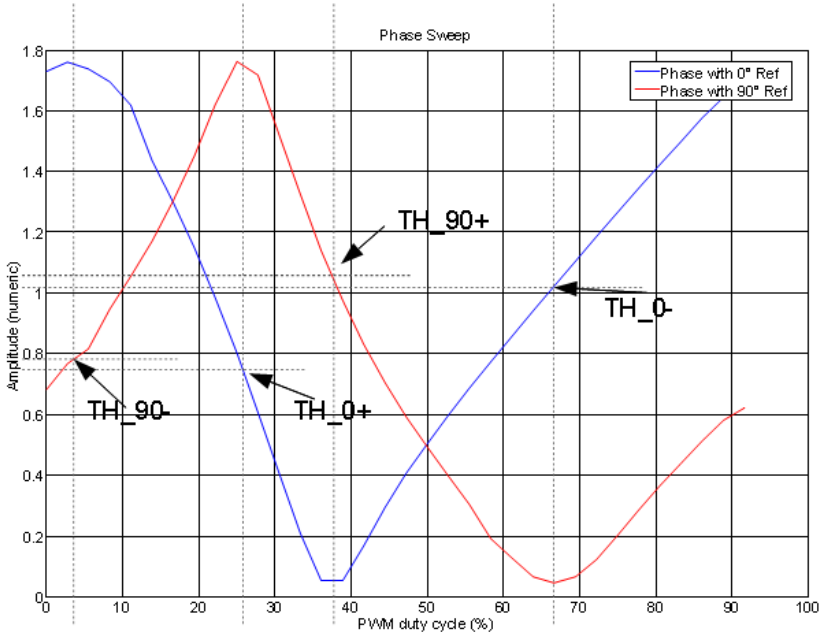

Figure 6.16: Phase Thresholds

used as compensation function and it is plotted in Figure 6.17. *Error* is the difference between the reference and the measured carrier amplitude.

$$compensation = 10^{-10} \cdot error^3 - 10^{-6} \cdot error^2 + 0.0077 \cdot error \tag{6.7}$$

The compensation function was calculated according to a set of fussy logic decisions. the compensation is given in duty cycle change of the PWM signal, and it depends on the amplitude difference between the reference and the actual amplitude of the carrier after the addition point.

Periodic Accumulator (Regulator) The regulator is basically an I regulator, nevertheless it functionality differs form the typical one. The regulator works with iterations, as already mentioned it works in some way with fuzzy logic. The logic is as follow:

- If the error in the loop is big compensate the phase of the signal greatly and vice versa.
- If the phase difference is negative compensate the phase in a negative direction and vice versa.

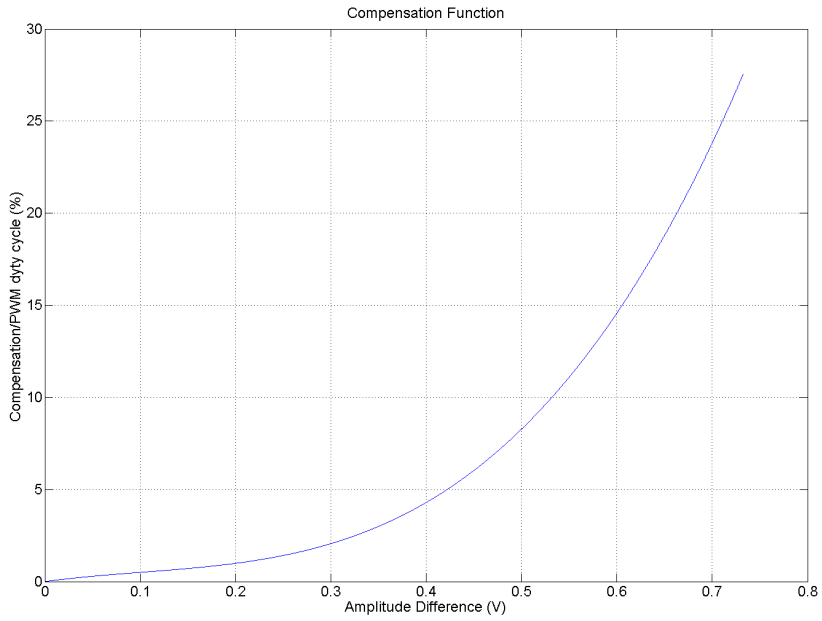

Figure 6.17: Plot of the Compensation Function

- In the next iteration the phase compensation is added to the one of the iteration before (accumulator principle). The phase difference is stored in every iteration.
- The output of the regulator is periodic, i.e. the phase compensation can just take values between -180° and 180°.

On every iteration the regulator tries to minimize the error and converges when the phase difference toggles constantly from -180° and 180°. In other words the error signal converges to 0, (see Figure 6.15). Results of the carrier suppressing circuit are shown in section 7.4.

Chapter 7

Evaluation and Results

This chapter presents the results of the optimizations and changes, realized in this work, applied to the UHF RFID systems.

7.1 Reconfigurable Reader

The test platform offers a flexible environment to test and implement new algorithms for UHF RFID systems. The digital processing elements are logic modules described in software. Most of the system elements are defined with programmable logic.

Advantages

- The digital processing elements are configurable and reusable.
- The digital processing elements can be used stand-alone or be included in a bigger system.
- New modules can be easily described and added to the system under test.
- Different receiver architectures can be tested parallel.

7.1.1 Digital Signal Processing Module for Reader-Prototype Development

Good results were obtained with the new approaches and the test-platform. Nevertheless the test platform presented in chapter 4 is suitable for algorithm test and development, but not for a final product. The system is complex and has a relative

high cost compare to RFID readers in the market. Therefore a digital signal processing (DSP) module for reader-prototyping was developed.

Concept

The goal is to have a modular system where the digital processing always takes place in the same module, only the analog module needs to be changed according to the system requirements. The DSP module should be flexible enough to cover all possible implementations. Refer to [52] for more information.

Characteristics

- *Processor:* The module is equipped with a Spartan 3^{TM} DSP [4] FPGA, which has the required amount resources, and it is optimized for DSP. The FPGA runs at 200 MHz.
- *Control:* There is a high performance microcontroller included in the module. The microcontroller has direct USB interface and a shares a fast bus communication interface with the FPGA.
- *Interface to the Analog Module:* The ADCs and DACs are in the analog module side, therefore the DSP modules have a fast digital interface for 4 16-bit parallel buses plus clocking signals.

Figure 7.1 shows a photograph of the DSP module. Figure 7.2 shows a photograph of the DSP modules (right) with a corresponding analog module (left) for a RFID HF systems.

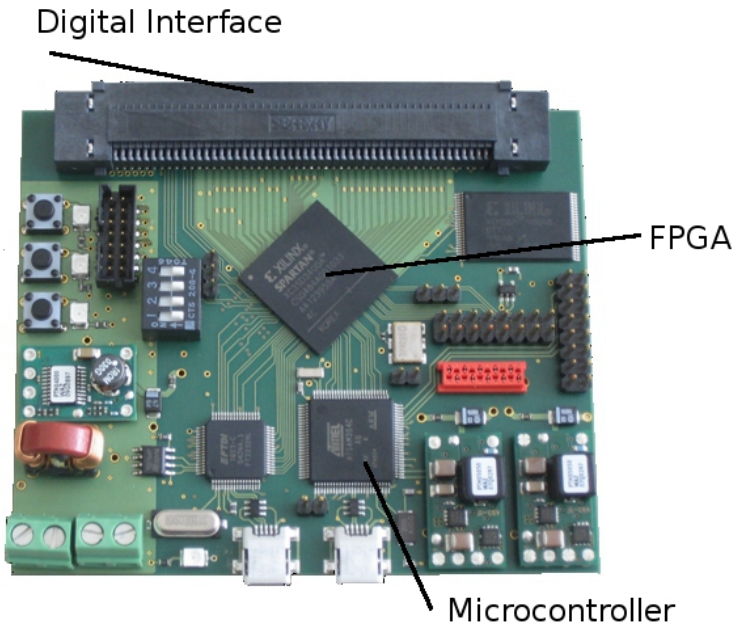

Figure 7.1: Photograph of the Digital Signal Processing Module

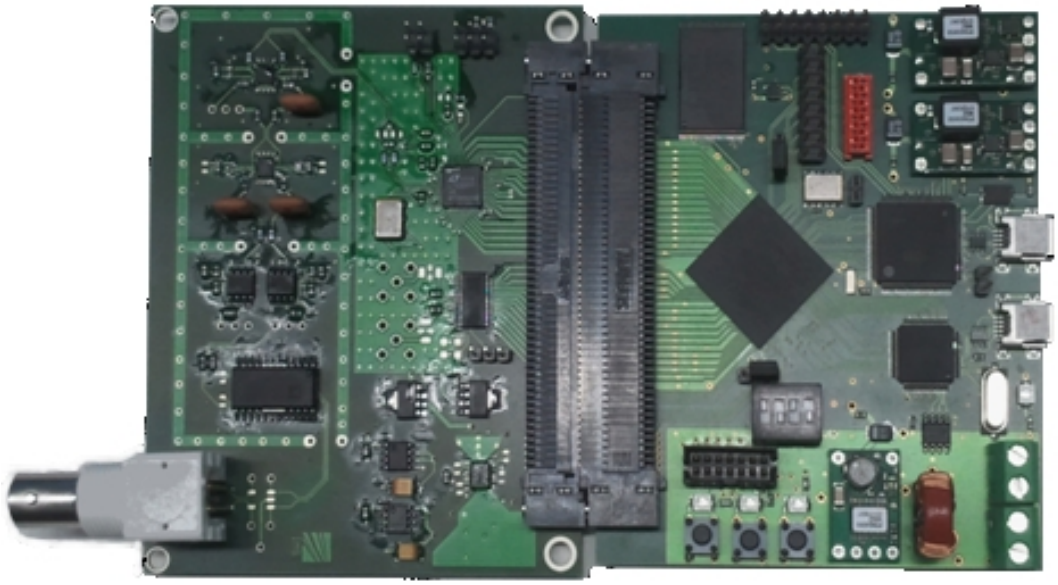

Figure 7.2: Photograph of the Digital Signal Processing Module and Fitting Analog Module

7.2 Under-sampling Approach

This section presents the results of applying the under-sampling scheme in UHF RFID systems. First the results of the simulation are presented, followed by a feasibility test. At last the scheme is implemented in the test platform and the results are presented as well.

7.2.1 Simulation

For the simulation the signal at the input of the demodulator, Figure 3.7 of section 3.2, is re-sampled with a frequency of 41.459 MHz for a $n = 41$ (see equation 5.5 and 5.6) and an FFT was taken to obtain its spectrum.

The Figure 7.3 shows the time signal in the top-left plot and the frequency spectrum in the bottom-left plot **before** undersampling, this last plot shows only the positive side of the spectrum. The carrier can be seen in the center and the side lobes corresponding to the backscatter signal.

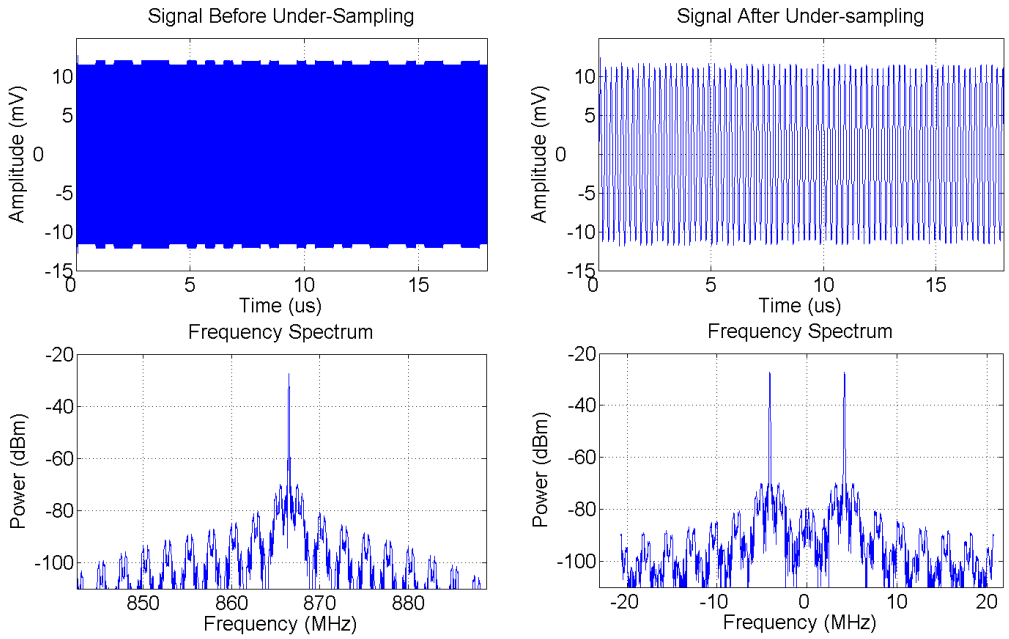

Figure 7.3: Signal after Undersampling

The same figure shows the time signal **after** the under-sampling in the top-right plot and the corresponding frequency spectrum in the bottom-right plot. By analyzing the spectrum it can be seen how the signal's spectrum has been shifted and how the

side lobs of the signal keep the same frequency offset as in the original signal, i.e. an IF signal is created. In the plot, the positive and the negative spectra can be seen since the new IF is quite smaller. The new frequency of the carrier signal (IF) can be determined by:

$$f'_x = \begin{cases} f_x - \frac{n}{2} \cdot f_s, & \text{for } n \text{ even} \\ \\ -(f_x - \frac{n+1}{2} \cdot f_s), & \text{for } n \text{ odd} \end{cases} \tag{7.1}$$

Where f'_x is the resulting frequency, after under-sampling, for a given original frequency f_x. In this case the resulting carrier frequency is 4.162 MHz. In Figure 7.3 can be seen how the frequency spectrum remains the same, the basic signal form does not change. The result is a bandpass image of the original bandpass signal at a lower frequency band, resulting in a signal easier to process.

7.2.2 Feasibility Tests

Before implementing the under-sampling scheme in UHF RFID systems, it was necessary to corroborate the results of the simulation. Using a signal generator, a circulator and an antenna, a CW (Continuous Wave) is radiated to a test tag. The test tag, explained in section 4.4, is programmed to send a continuous message. The received signal can be seen directly on an oscilloscope. Figure 7.4 shows the measurement block diagram.

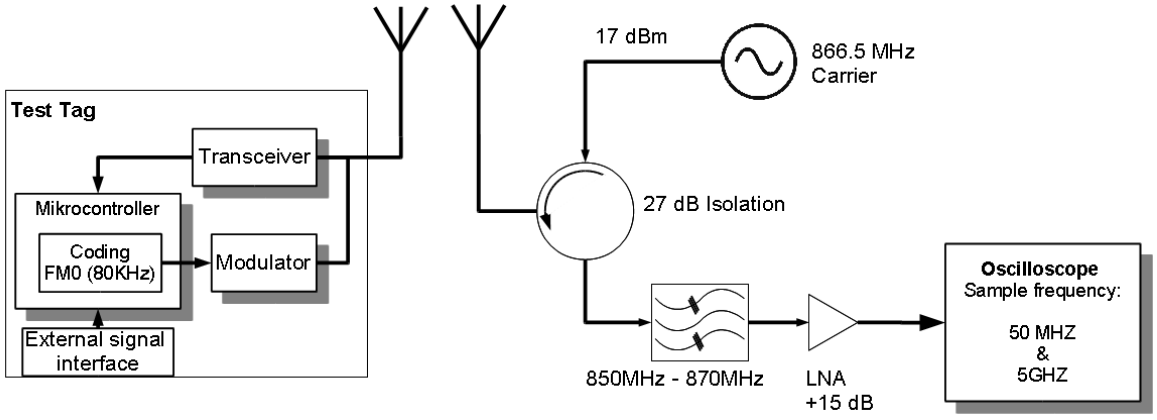

Figure 7.4: Measurement Block Diagram

By changing the sample frequency of the oscilloscope the received signal is either oversampled ($f_s >> f_{max}$) or under-sampled. As reference the sample frequency of the oscillator was set at 5 GSPS in order to oversample the signal. In Figure 7.5 can be seen the time signal and the corresponding FFT. The modulating signal can be seen in the envelope of the time signal and on the side lobes of the FFT as well.

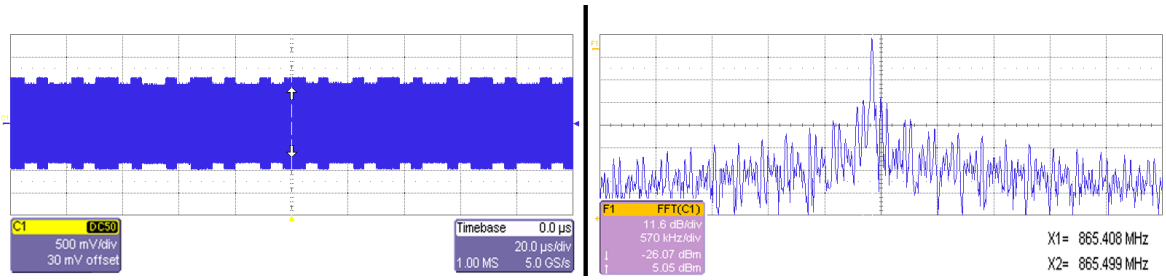

Figure 7.5: Oscilloscope View with Oversampling

To test the feasibility of the under-sampling for UHF RFID the sample frequency of the oscilloscope was set at 50 MSPS. In Figure 7.6 can be seen the time signal and the corresponding FFT. The modulation signal can still be seen in the envelope of the time signal and on the side lobes of the FFT as well. The under-sampling process does not destroy the information signal.

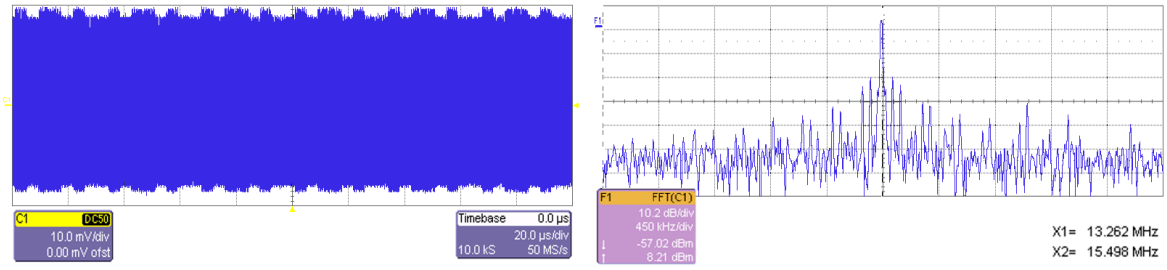

Figure 7.6: Oscilloscope View with Undersampling

By comparing both Figures 7.5 and 7.6 it can be seen that the under-sampled signal presents a higher noise level than the oversampled one. This is the main disadvantage of under-sampling and is due to the overlapping from many alias images over each other [70]. The noise of each image added to noise of the other ones degrades the SNR (Signal to Noise Ratio) of the signal. Section presents 5.2 a way to overcome this disadvantage.

7.2.3 Hardware Implementation

The results of the hardware implementation are presented here. As already mentioned, the new sampling scheme was implemented using the test platform. Figure 7.7 shows the block diagram of the measurement. Two results are presented: the received signal digitized using the under-sampling scheme and a received signal sampled after a frequency shift element (mixer) for reference. In the last case the sample frequency is much bigger than frequency of the signal (over-sampling). The carrier decoupling circuit used is the double circulator element shown in 4.2.1, nevertheless it is represented as a single circulator in Figure 7.7 for simplicity.

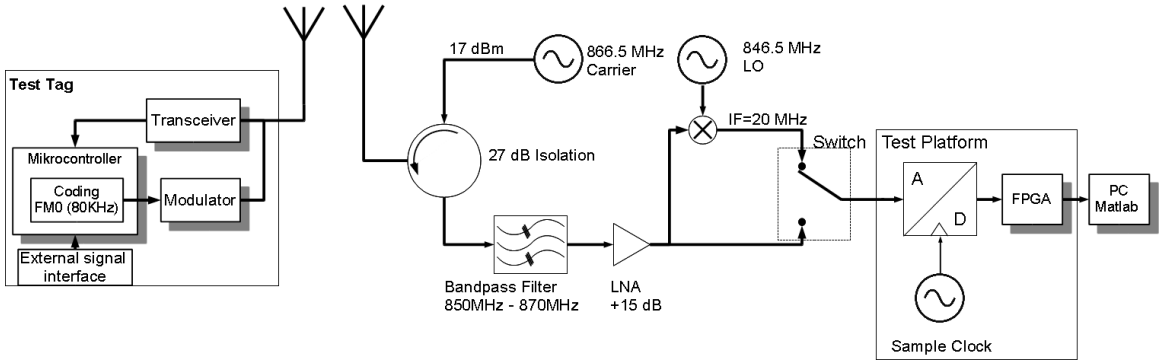

Figure 7.7: Hardware Implementation Block Diagram

Figure 7.8 shows the time plot of the signal after the mixer on the top-left and the corresponding spectrum on the bottom-left; the sample frequency used is 866.5 MHz. The under-sampled signal is time plotted in the top-right of the figure and its corresponding spectrum on the bottom-right; the sample frequency used is 42 MHz (see section 7.2.1).

For this measurement the distance between the tag and the reader is 1 m. This allows us to see the information signal in the envelope of the time domain plot.

7.2.4 Analysis

From Figure 7.8 it can be seen that:

- The information signal is not destroyed by under-sampling. The side lobs can be clearly seen.
- The inter modulation products and harmonics present on the signal taken after the mixer do not appear on the under-sampled one.

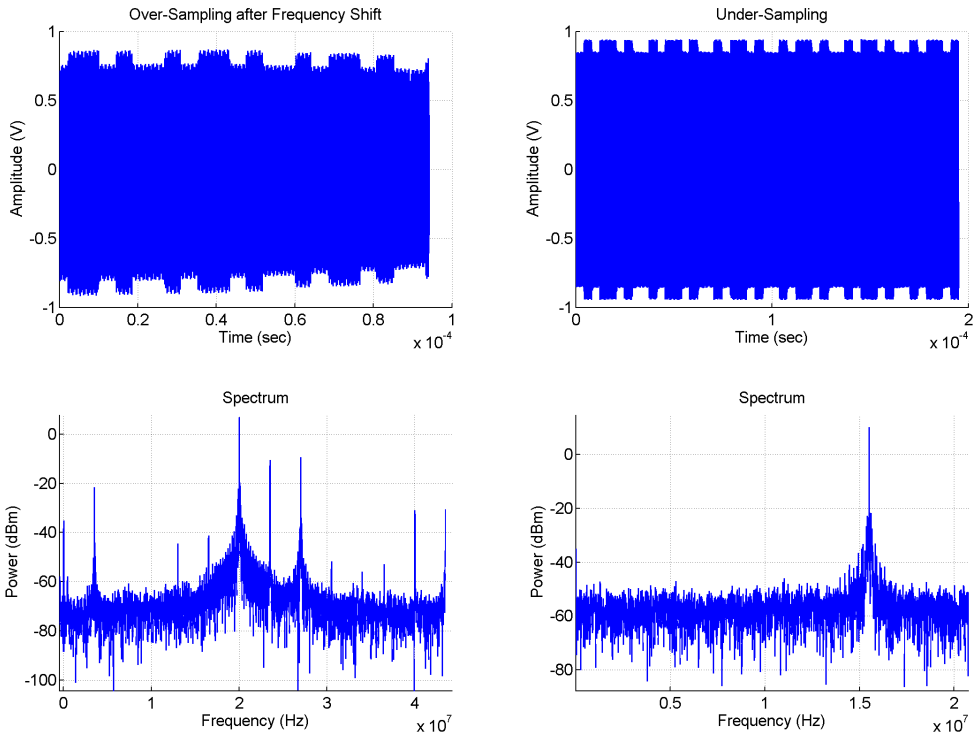

Figure 7.8: Sampled Signals

- The resulting signal after the under-sampling is frequency shifted. This is very practical, since the digitization and mixing takes place in the same process
- The noise level on the under-sampled signal is higher than the other one. This is due to the overlapping of replicas generated by the under-sampling

Advantages

- The signal is in the digital domain in an earlier state.
- The signal can be frequency shifted and/or decimated in the digital domain.
- The signal is not distorted by physical filters or the analog bandwidth of analog elements
- No mixer is necessary, therefore less analog components and lower system cost.

Disadvantages

- The SNR of the signal decreases. Nevertheless the analog mixing process is a non-ideal process as well, noise and nonlinear effects take place in the process.
- The ADC requirements are quite high. It should have enough bandwidth to accommodate the RF signal.

Outlook: The limits of the bandpass filter can be chosen to cover the complete SRD band used by UHF RFID systems. The further filtering of every channel could take place in the digital domain. This approach allows a wider use of the RFID System for any country norms.

7.3 Bit-Error-Rate Comparison Between Coding Schemes

This section shows the results of using the full symbol correlation presented in section 5.3 and the new coding scheme of section 5.4. First the results of a simulation are presented, followed by a hardware implementation in the test platform.

7.3.1 Simulation

The graphic in Figure 7.9 shows the resulting BER of the receiver according to its SNR. It is important to note that the chip length was normalized to one half of the time period of the FM0 symbol. Therefore the band width of all coding symbols is the same, only the symbol length changes. In this way the performance of each symbol form can be compared to the performance of the others.

7.3.2 Measurement

Figure 7.10 shows the results of the measured BER test of the different coding schemes. Note: In Figures 7.9 and 7.10 GC stands for Gold Code and L for length.

7.3.3 Analysis

From Figure 7.10 it can be seen that the performance of the Miller coding scheme is worse than it was shown at the simulation. By the PN coding scheme the BER

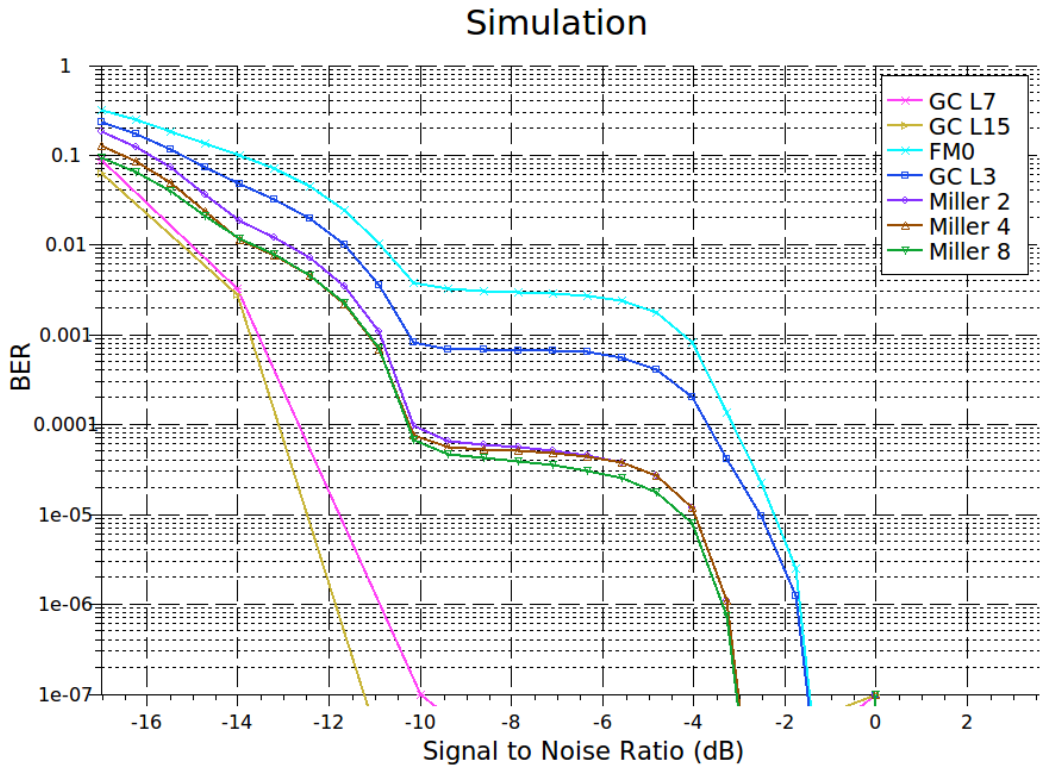

Figure 7.9: BER Results of the Simulation [35]

does not converge to zero as fast as by the simulation. Important is the notorious difference between Miller and PN codes, the hardware implementation shows a bigger difference than the simulation. The unexpected straightening of the curves at higher SNR values could be caused by bit errors that are introduced by the hardware and the imperfections in the implementation.

Even though the simulation was made as close as possible to the implementation, there are some differences between the measured and simulated results. Important is the demonstration of the advantages of using gold sequences to encode information over the usage of the RFID standardized codes [35].

Comparison: It is important to point out that the comparative is relative, it only compares the performances of the coding schemes to each other. All possible system influences are equal to all tests, which leaves only the SNR of the signal and the BER. This applies for both the simulation and the implementation. It can be seen that the

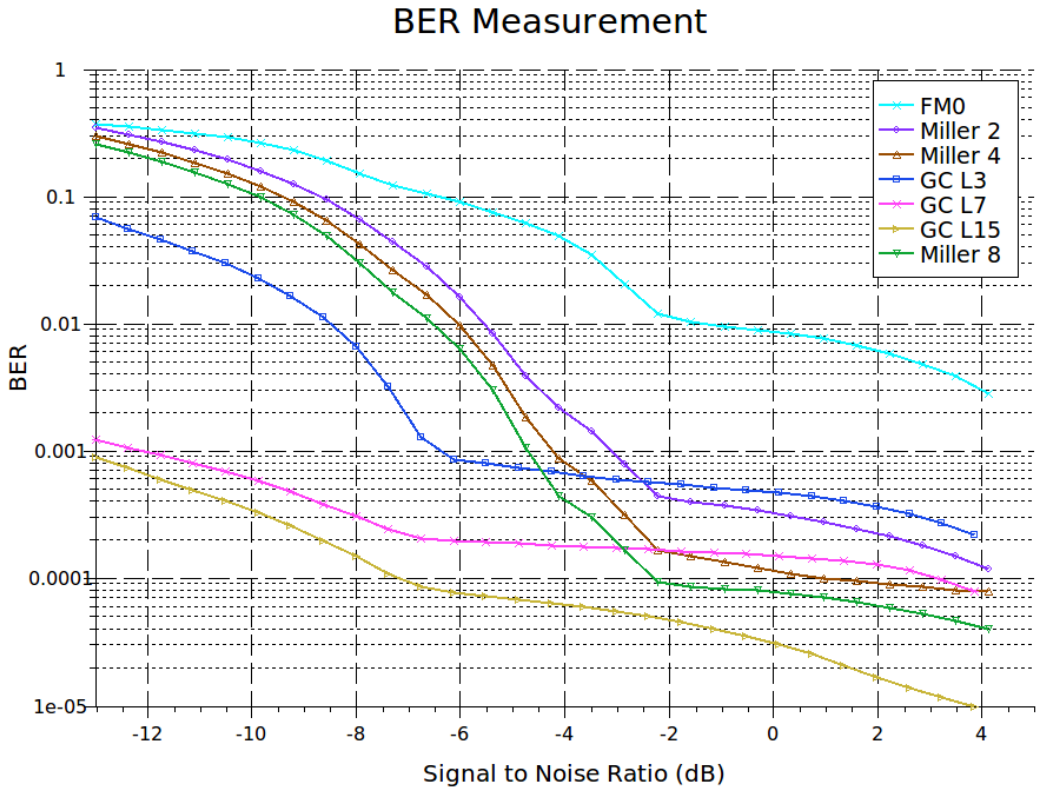

Figure 7.10: BER Results of the Measurement [35]

Miller 8 symbols have a better performance than the Miller 4, in the same way this last one has a better performance than the Miller 2 and so on. This is due to the symbol length, the longer the symbol the more the SNR is improved by the full correlation receiver, see section 5.3 .

It was shown that the gold encoded messages were received with less errors than the Miller-coded ones. This is due to the orthogonality of the symbols as well as the characteristics of the PN codes, these make them less susceptible to environment influences.

The form of PN code itself presents direct advantages, the symbols are orthogonal to one another which decreases the bit-error-rate. If one half of the FM0 symbol is considered as a chip in the Miller coding, the two codes can be compared according to their chips-per-bit rate. At miller 8 one bit is sent using 16 chips. At its comparable gold sequence 3 bits can be sent using 15 chips, that is 5 chips per bit instead of 16

chips per bit of the Miller 8 coding scheme.

7.3.4 Bit-Error-Rate Improvement on Fading Sensitive Environments

As already shown the BER can be improved by using a different channel coding scheme for the tag-to-reader communication. The PN coding scheme is more robust than the standardized FM0 and Miller codes. This brings a great improvement in UHF RFID Systems.

The implementation of the coding logic at the tag is relatively easy. Nevertheless one disadvantage of this procedure is the increase of complexity at the reader. Each sequence requires a corresponding correlator at the reader, and by extending the length of the sequence the resources required by the correlator increase as well.

7.4 Improvement by High Isolated Carrier Suppressing Circuit

The carrier isolation is of critical importance in RFID systems. Increasing this factor brings many advantages for the system:

- With a lower carrier level the signal can be better amplified without reaching saturation, hence a higher sensitivity is reached. Less dynamic range required for the ADC.
- The SNR of the signal is significantly improved ca. 40 dB. (see Figure 7.11). The improvement is made by the fact that the carrier suppression reduces the power level of the carrier and with it the phase-noise of the carrier. The information signal is not affected by the carrier suppression.
- The complexity of the signal processing at the reader is reduced.

Figure 7.11 shows a measured frequency spectrum of the received signal in a UHF RFID reader by using the new carrier suppressing circuit. The peak in the center of the plot is the carrier signal which still couples in the receiver. The peaks beside are the side lobs of the information signal, the difference between carrier and information signal is now approx. 20 dB. Figure 7.12 shows a comparative of two frequency spectra.

The line in blue is the signal received with a single circulator, the line in pink is the signal received by using the high isolated carrier suppressing circuit.

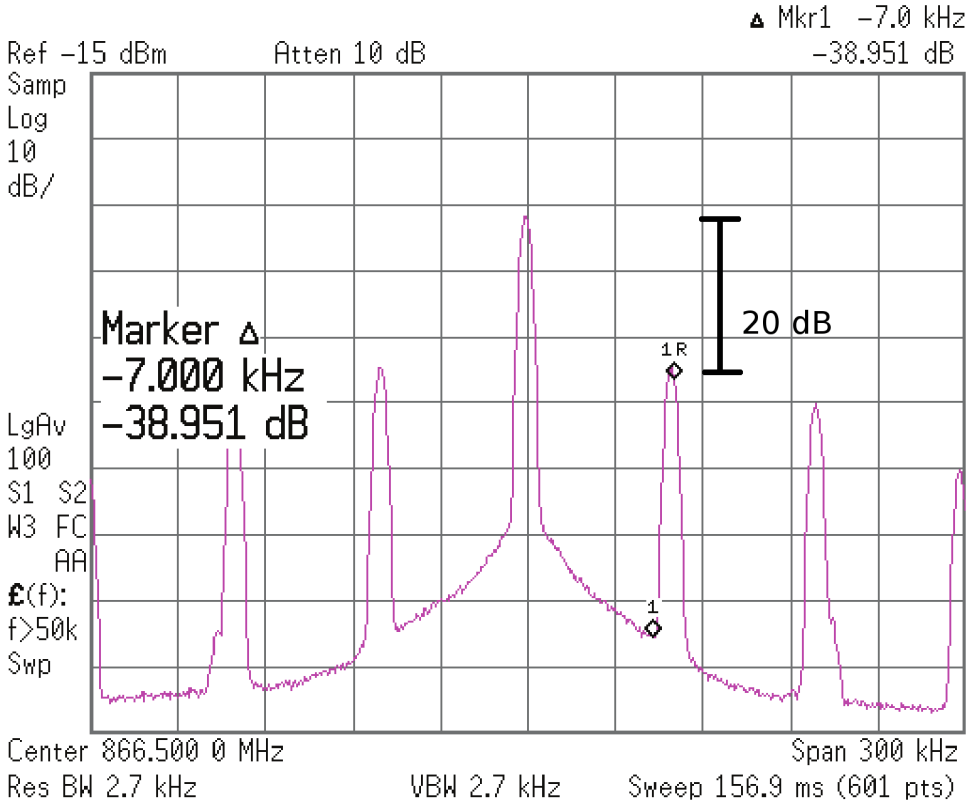

Figure 7.11: Frequency Spectrum of the Received Signal [61]

The isolation has been improved to ca. 50dB compared to the 20 dB of a single circulator. It can be seen how the carrier level is smaller together with its phase noise. The noise level around the carrier is reduced, hence the side lobs of the information signal emerge out of the noise floor. The figure shows a power difference of approx. 20 dBc between the carrier and the side lobs.

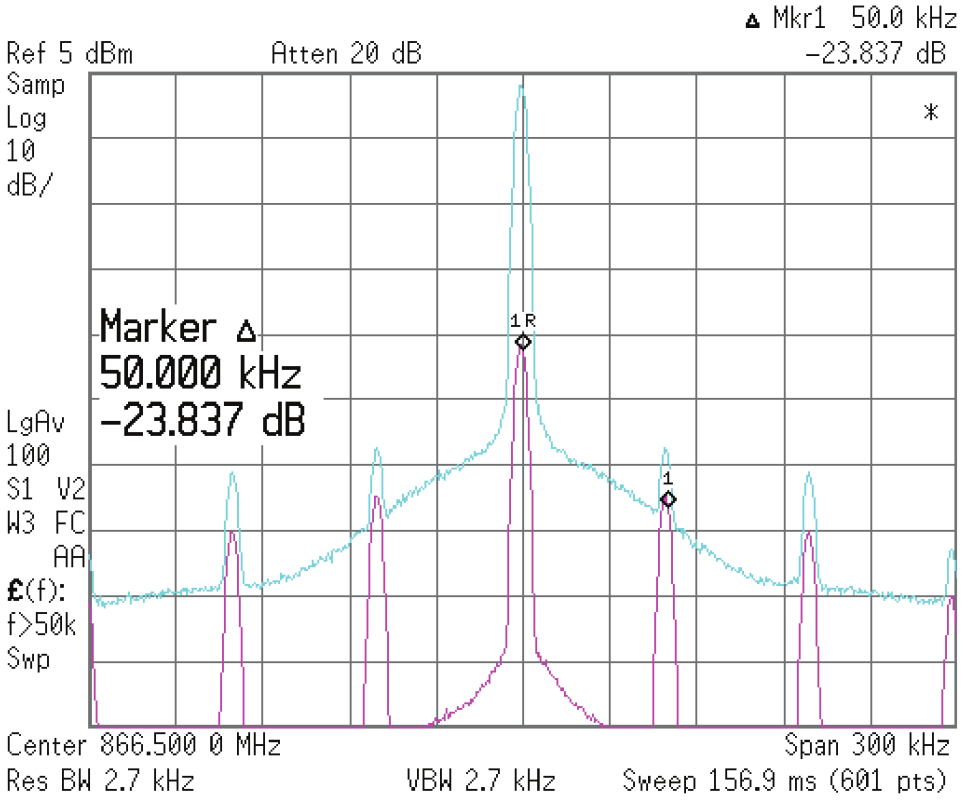

Figure 7.12: Comparing Between Carrier Suppressing Circuits [61]

7.5 State-of-the-Art Comparison

This section presents some tests that were made in order to compare the performance of the novel RFID system presented in this work, from now on called RUT (Reader Under Test), with some state-of-the-art devices. The topics considered are receiver architecture, and full symbol correlation; the PN coding and the carrier suppression can not be used in this comparison since they are not standard elements of UHF Systems, their improvements are considered separately. The readers used are:

Intel™ Reader: This is a reader based on the UHF RFID transceiver IC from Intel™(now Impinj™). The reader is basically an evaluation board for the IC, it offers some flexibility on the high frequency block, e.g. it can be configured in monostatic or bystatic mode among other parameters. It also offers some messing points directly at the high frequency circuitry. This reader was chosen because many of the readers on the market are based on this IC.

FEIG™ Long Range Unit 2000: This is a reader built with discrete components and a digital processing unit. The reader is an out-of-the-box product and offers less or none flexibility for extra configuration or measurements. This reader was chosen because it is on of the best long range readers on the market.

Tag: The tag used for the measurements is a reference tag form the company Voyantic™. Out of a conformance test system.

7.5.1 Read Range

The first test is a read range test. The measurements were made in an anechoic chamber, the antennas and connections are the same for all the devices. The position of the antennas are fixed, the distance from the antennas to the tag is increased after every read try until the reader can not retrieve the information of the tag. The RUT and the Intel reader work in monostatic mode, in this way the transmitter and the receiver can be handled separately. The FEIG reader can not be used in monostatic mode. The RUT was tested with the 12-bit using under-sampling and with the 16-bit ADC with a mixing step before; the IF used is 10 MHz. The measurement parameters are as followed:

- *Power*: 0.5 Watts or 27 dBm
- *Carrier Frequency*: 866.5 MHz
- *BLF*: 265 KHz
- *Up-link Coding*: Miller 4
- *Down-link Data Rate*: 40 KHz
- *Down link Modulation*: DSB-ASK
- *Sample Frequency (just for the RUT)*: the sample frequency chosen for the 16-bit RUT is 100 MHz because it is the maximum frequency allowed by the ADC. For the 12-bit RUT a sample frequency of 292 MHz is chosen, this value corresponds to an n=5, see section 7.2.1. Values close to 300 MHz give better sampling results, see section 5.2.

The parameters need to be common to all devices under test. All the given values were chosen according to this criteria. Table 7.1 shows the results of the read range measurement, the successful reads are mark with "OK".

The results show that almost all readers were able to read up to 2.5 meters, the read range is mainly limited by the tag's energy range. The tag requires a certain amount of signal power in order to provide its circuitry with energy, in this case the tag does not work after 2.5 meters. The FEIG reader can read the tag until 2.4 m the same as the RUT working with the 12-bit ADC and under-sampling.

The main reasons why the 16-bit RUT is better than the 12-bits RUT is because of the higher dynamic range of the 16-bits ADC and the extra noise added by under-sampling the signal.

Distance(cm)	FEIG	Intel	IMS RUT 16-bit ADC	IMS RUT 12-bit ADC
50	OK	OK	OK	OK
70	OK	OK	OK	OK
90	OK	OK	OK	OK
110	OK	OK	OK	OK
130	OK	OK	OK	OK
150	OK	OK	OK	OK
170	OK	OK	OK	OK
190	OK	OK	OK	OK
210	OK	OK	OK	OK
220	OK	OK	OK	OK
230	OK	OK	OK	OK
240	OK	OK	OK	—
250	—	OK	OK	—
260	—	—	—	—
270	—	—	—	—

Table 7.1: Results of the Read Range Test

7.5.2 Sensitivity

This test shows the capability of a reader to retrieve information out of a signal with small power level and buried in noise. The measurements were made in an anechoic chamber, the antennas and connections are the same for all the devices this test was made just for the Intel and the RUT readers. The RUT was tested with the 12-bit using under-sampling and with the 16-bit ADC with a mixing step before; the IF used is 10 MHz. To measure the signal level is not an easy procedure, specially since it is not possible to measure the baseband signal inside the Intel™ IC. Therefore the sensitivity was tested in the following way:

- Since the transmitter and the receiver paths are independent (bistatic configuration) it is possible to influence the signal before the transmitter.

- The systems are influenced by placing some attenuators between the antenna and the receiver.
- As the attenuation increases, the signal level decreases. In the same way the more attenuation the more noise is added to the signal.
- The measurement parameters are the same as for the read range test. Table 7.2 shows the results of the sensitivity test.

Attenuation (dB)	**Intel**	**IMS RUT 12-bit ADC**	**IMS RUT 16-bit ADC**
0	OK	OK	OK
3	OK	OK	OK
9	OK	OK	OK
15	OK	OK	OK
21	OK	OK	OK
28	OK	OK	OK
29	Error	OK	OK
30	—	OK	OK
31	—	OK	OK
32	—	OK	OK
33	—	Error	OK
34	—	—	OK
35	—	—	OK
41	—	—	OK
46	—	—	OK
47	—	—	Error
48	—	—	Error
49	—	—	—
50	—	—	—

Table 7.2: Results of the Sensitivity Test

In Table 7.2 the successful reads are marked with "OK", if the ID was read with some bit errors the field is marked with "Error". The RUT shows a quite higher sensitivity than the Intel^{TM}reader. The are some factors that explain the difference:

- The noise added by the direct down converter in the Intel reader reduces the sensitivity of the receiver. This architecture presents the following problems:
  - Self mixing: The local oscillator signal couples into the input of the mixer creating a time variable DC offset that increases the noise level of the signal.
  - 1/f noise: The noise increasing due to the self mixing factor is indirectly proportional to the frequency.
- In the RUT the demodulation is done in the digital domain. This is done in the digital receiver presented in section 5.2.
- The lowpass filter after the demodulator is a 4th order filter. The FIR filter in the receiver has a faster roll-off, this limit the bandwidth of the signal in a better way and with it the noise. The lowpass filter in the digital receiver reduces the bandwidth of the signal more efficiently.
- The receiver filter uses the complete symbol form as correlator, see section 5.3. The longer the correlator the more SNR improvement is made.
- The bandwidth of both RUT receivers is higher than the bandwidth of the Intel^{TM} reader, this allows more of the signal energy to be used. The bandwidth of the 16-bit RUT is 50 MHz and the one of the 12-bit is 73 MHz after the first by 2 decimation, (using the corresponding digital receiver).

The 16 bit receiver has a higher sensitivity than the 12 bit receiver, this can be explained by the following facts:

- The 16 bit ADC has a higher dynamic range: 24 dB more than the 12 bit ADC. See equation 5.7.
- The under-sampling technique adds extra noise to the signal, approx. 7 dB in this case. See equation 5.8, calculated for $n = 5$.

Figure 7.13 shows the frequency spectrum of the signal delivered by the antenna at different attenuations. The plots show just the positive side of the frequency spectrum, the highest peak is the carrier, the side lobes are the information signal. The top-left shows the frequency spectrum of the received signal without attenuation, the top- right plot with an attenuation of 10 dB, the bottom-left plot with an attenuation of 30 dB and the bottom-right with and attenuation of 46 dB. It can be seen how in the bottom-right plot the side lobes of the information signal are buried in the noise floor. It can also be seen some low-frequency disturbing signals that need to be filter before the demodulator, nevertheless this filtering does not take place in this work.

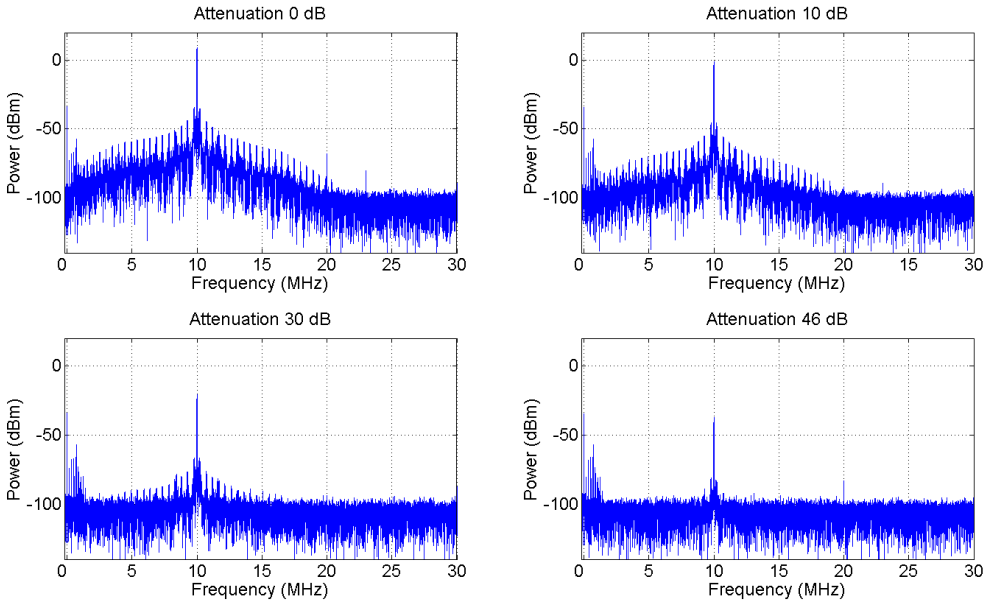

Figure 7.13: Frequency Spectrum of the Received Signal at Different Attenuation

Chapter 8

Conclusion

8.1 New System Approach

This work presents optimizations and improvements for UHF RFID systems. Everything was implemented and tested in a self-developed test platform. Most of the signal processing elements are software-defined. One of the goals was to create a flexible system where new ideas could be evaluated rapidly and at the same time to be included in a standard system without a big effort. Therefore the software based system was chosen. The result is a high performance system that is able to communicate and work with standard UHF RFID tags. Great improvements have been achieved in the data recovery performance, hence higher read range and system flexibility.

8.2 Carrier Suppression

A big improvement was achieved with the presented active and digital controlled circuit. This circuit can be used by any UHF RFID system with separate TX and RX ports.

8.3 Optional System

Optionally, a big system improvement could be realized by changing the line coding scheme of the UHF RFID tags. It was demonstrated how the BER can be reduced drastically by using PN-codes instead of the standard FM0 and Miller. Furthermore data rate is increased by using the orthogonality of the codes to send more than one bit per symbol. Even though this line coding scheme is not part of the UHF RFID

standards it could be part of future updates. Nevertheless this line coding scheme could be used for application specific tags, e.g. sensor transponders that are typically placed in high reflective environments where the standard UHF RFID systems does not work anymore. The main changes to be considered are: the encoding of the digital data in the tag and the receiver architecture at the reader.

8.4 Outlook

- The test platform can be used for further investigation projects, new algorithms can be implemented and tested without the need of extra hardware.
- The new algorithms, once tested, can be easily ported into the digital processing module in order to reduce the time-cost of product development.
- The processing elements are modular and can be reused, for other RFID systems.
- The test platform can be used for testing not only the UHF RFID systems but HF and LF systems as well.

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